CYD2500

4GSPS 12 位射频采样模数转换器（ADC）

1. 特性

- 分辨率：12-bit，无失码（no missing code）
- 采样率：
  4GSPS（单通道），2GSPS（双通道）
- 通道数：1 或 2
- 输入电压范围[Vpp,diff]：0.8V (typ)，1V (max)
- 模拟输入带宽(-3dB)：3.0 GHz
- 误码率（Code error rate）：< 10-15
- 积分非线性 INL：-1.3 / +1.3 LSB @ 180 MHz
- 微分非线性 DNL：
  -0.32 / +0.40 LSB @ 180 MHz
- 信噪比 SNR @ -1 dBFS：
  52.1 dBFS (0.8Vpp)，53.6 dBFS (1.0Vpp)
- 无杂散动态范围 SFDR @ -1 dBFS：
  75.8 dBFS (0.8Vpp)，74.4 dBFS (1.0Vpp)
- 有效位 ENOB @ -1 dBFS：
  8.4b (0.8Vpp)，8.6b (1.0Vpp)
- 16 通道 JESD204B 输出，最大通道速率 10.0Gbps，支持 8b/10b 编码，支持子类 1 确定性延迟
- 可选数字下变频器(DDC)：
  实数输出支持 1x,2x,3x,4x,6x,8x,12x,16x,24x,32x,48x,64x 抽取比例
  复数输出支持 2x,4x,6x,8x,16x,24x,32x,48x,64x,96x,128x 抽取比例
  每个 DDC 均具有四个独立的 48 位 NCO，支持快速调频
- 模拟输入通道过压保护
- 片内温度二极管
- 低功耗：2.0W
- 封装：FCBGA196（12mm x 12mm）
- 工作温度（结温）：-40 to 115°C

2. 应用

- 示波器和宽带数字转换器
- 宽带通信系统
- 高速数据采集
- 通信测试仪（802.11ad，5G）
- 射频采样软件定义无线电（SDR）
- 光谱测量

3. 概述

CYD2500 是一款 12 位、高速射频采样模数转换器（ADC），单通道模式下的最大采样率为 4GSPS，双通道模式下每个通道的最大采样率为 2GSPS。单通道或者双通道工作模式可在线编程配置，可用于开发灵活的硬件，以满足高通道数或宽瞬时信号带宽应用的需求。CYD2500 采用高速 JESD204B 输出接口，工作温度（结温）支持 -40 to 115°C，芯片封装为 FCBGA196（12mm x 12mm）。

4. 订购指南（Orderable Information）

表 1 订购信息

物料编号	工作温度范围	等级类型	封装
CYD2500BAI	-40℃-115℃	工业级	FCBGA196

5. 功能框图

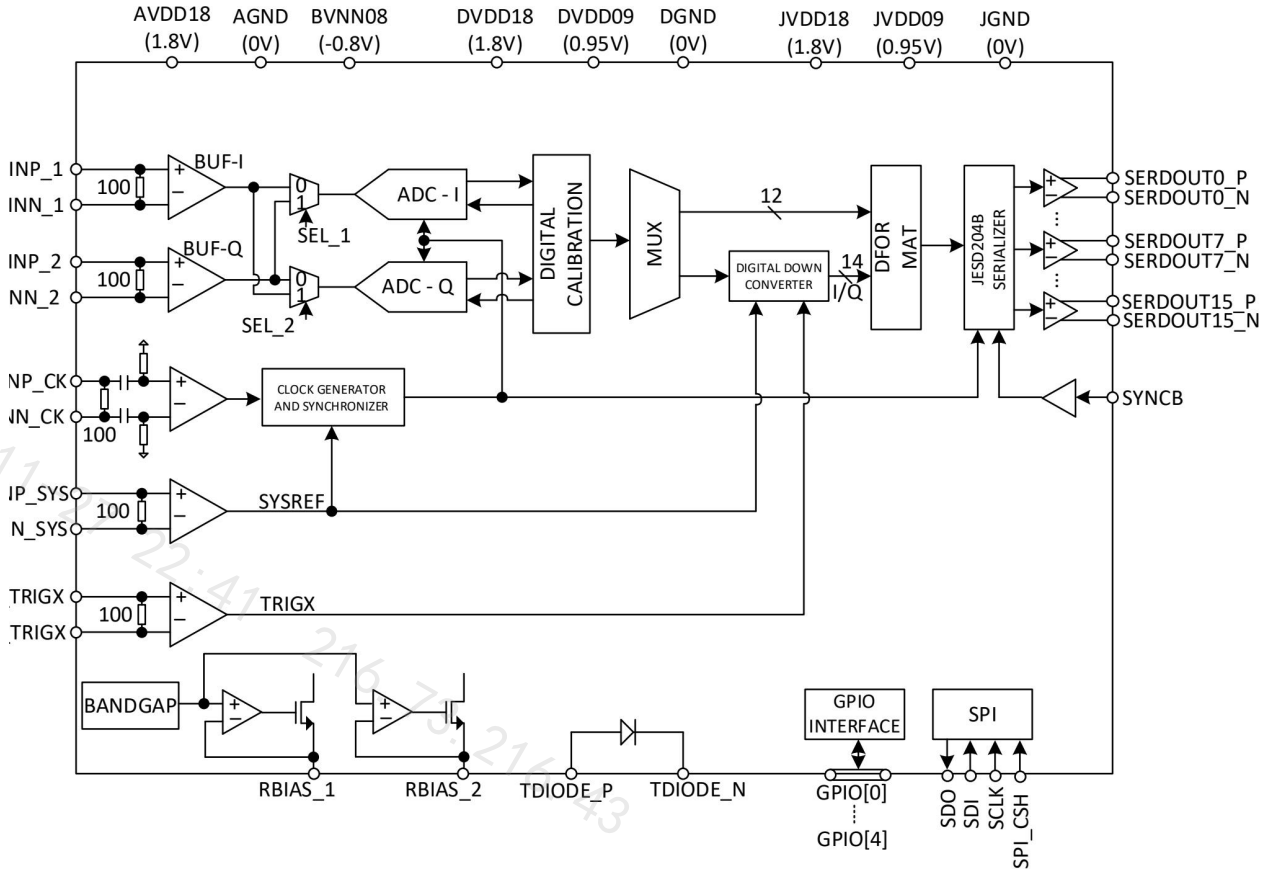

图 1 功能框图

6. 引脚配置和功能描述（Pin Configuration and Functions）

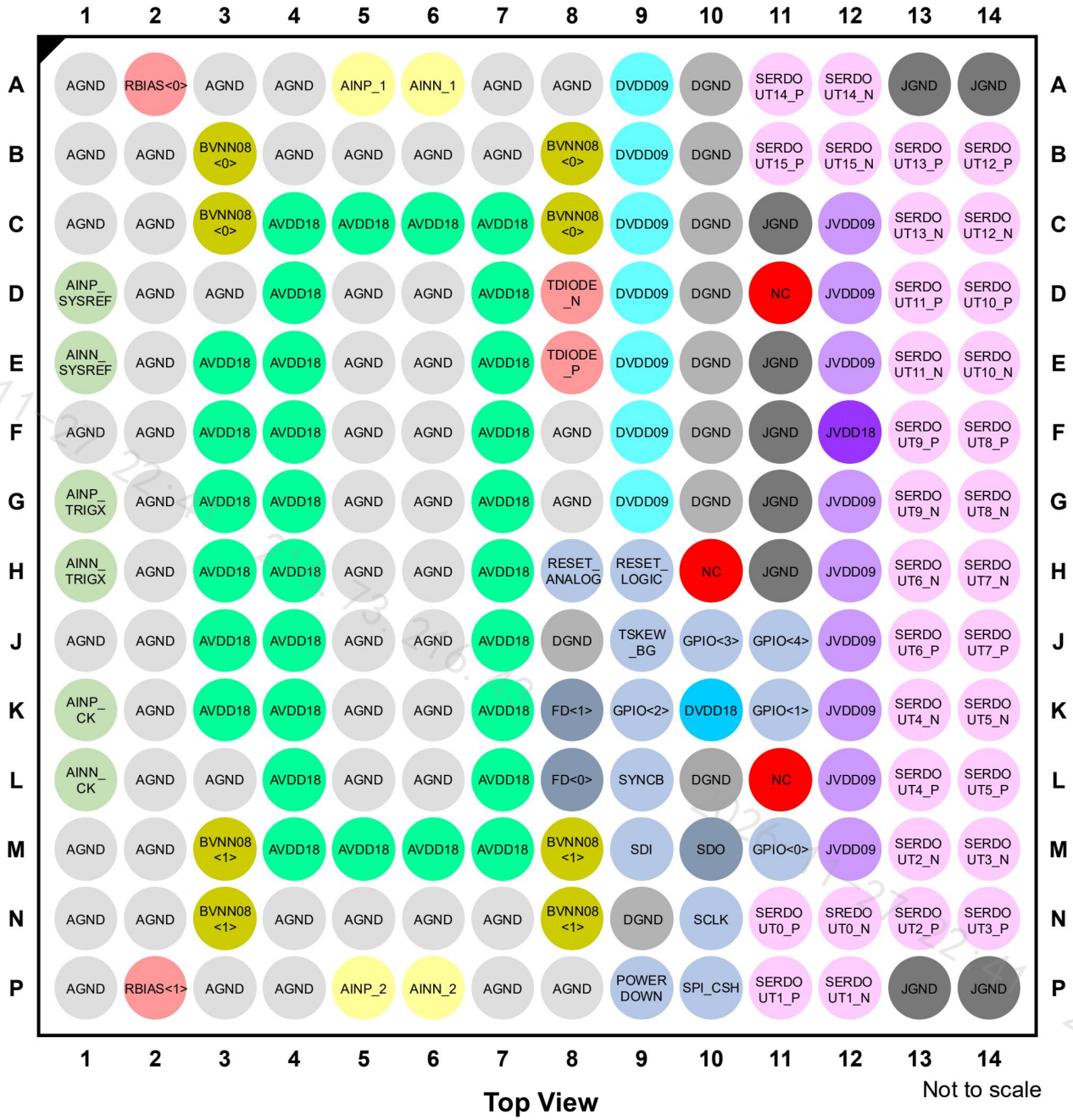

图 2 196-Ball Flip Chip BGA

表 2 引脚功能（Pin Functions）

管脚序号	管脚名	类型	功能描述
A2, P2	RBIAS<0> RBIAS<1>	输入	每个管脚接 12k 电阻到地。用于产生模拟电路内部参考电流。 注意 12k 电阻必须是高精度低温票电阻(建议采用 0.1%精度，温漂小于 25ppm/°C)
A5	AINP_1	输入	双通道模式：第一模拟通道差分输入的正输入（I-channel） 单通道模式：默认模拟通道差分输入的正输入（I 或者 Q channel） 它内接 50 欧姆电阻，支持 DC 或者 AC 耦合。请注意，该管脚必须满足输入共模电压范围及摆幅的要求。 默认状态下为单通道模式的模拟输入接口。
A6	AINN_1	输入	双通道模式：第一模拟通道差分输入的负输入（I-channel） 单通道模式：默认模拟通道差分输入的负输入（I 或者 Q channel） 它内接 50 欧姆电阻，支持 DC 或者 AC 耦合。请注意，该管脚必须满足输入共模电压范围及摆幅的要求。 默认状态下为单通道模式的模拟输入接口。
P5	AINP_2	输入	双通道模式：第二模拟通道差分输入的正输入（Q-channel） 单通道模式：可选模拟通道差分输入的正输入（I 或者 Q channel） 它内接 50 欧姆电阻，支持 DC 或者 AC 耦合。请注意，该管脚必须满足输入共模电压范围及摆幅的要求。 需要通过 SPI 才能切换为单通道模式的模拟输入接口。
P6	AINN_2	输入	双通道模式：第二模拟通道差分输入的负输入（Q-channel） 单通道模式：可选模拟通道差分输入的负输入（I 或者 Q channel） 它内接 50 欧姆电阻，支持 DC 或者 AC 耦合。请注意，该管脚必须满足输入共模电压范围及摆幅的要求。 需要通过 SPI 才能切换为单通道模式的模拟输入接口。
D1	AINP_SYSREF	输入	SYSREF 差分输入信号（正端），用于同步多 ADC 芯片数据时序给 FGPA。它内接 50 欧姆电阻，支持 DC 或者 AC 耦合。请注意，该管脚必须满足输入共模电压范围及摆幅的要求。
E1	AINN_SYSREF	输入	SYSREF 差分输入信号（负端），用于同步多 ADC 芯片数据时序给 FGPA。它内接 50 欧姆电阻，支持 DC 或者 AC 耦合。请注意，该管脚必须满足输入共模电压范围及摆幅的要求。
G1	AINP_TRIGX	输入	触发器(Trigger) X 差分信号(正端)，用于 DDC 模块的频率跳变。它内接 50 欧姆电阻，支持 DC 或者 AC 耦合。请注意，该管脚必须满足输入共模电压范围及摆幅的要求。
H1	AINN_TRIGX	输入	触发器(Trigger) X 差分信号(负端)，用于 DDC 模块的频率跳变。它内接 50 欧姆电阻，支持 DC 或者 AC 耦合。请注意，该管脚必须满足输入共模电压范围及摆幅的要求。
K1	AINP_CK	输入	主时钟差分信号(正端)，该管脚给芯片提供主时钟，芯片内部通过 50 欧姆电阻 AC 耦合，但该管脚必须满足输入共模电压范围及摆幅的要求。
L1	AINN_CK	输入	芯片内部通过主时钟差分信号(负端)，该管脚给芯片提供主时钟，50 欧姆电阻 AC 耦合，但该管脚必须满足输入共模电压范围及摆幅的要求。
E8	TDIODE_P	输入	温度二极管正（阳极）连接，通过外置温度传感器来监视芯片结温。该管脚没被使用时，请悬空。
D8	TDIODE_N	输入	温度二极管负（阴极）连接，通过外置温度传感器来监视芯片结温。该管脚没被使用时，请悬空。
B3, B8, C3,C8, M3,M8,N3, N8	BVNN08<0> BVNN08<1>	输入	模拟电路负电源供电管脚。它们连接到外部负 LDO 电源，该电源必须满足规范中的负电位和漏电流要求。
C4, C5, C6, C7, D4, D7, E3, E4, E7, F3, F4, F7, G3, G4, G7, H3, H4, H7, J3, J4, J7, K3, K4, K7, L4, L7, M4, M5, M6, M7	AVDD18	输入	1.8V 模拟 I/O 电源

管脚序号	管脚名	类型	功能描述
A1, A3, A4,A7, A8, B1,B2, B4, B5,B6, B7, C1,C2, D2, D3, D5, D6, E2,E5, E6, F1,F2, F5, F6,F8, G2, G5,G6, G8, H2,H5, H6, J1, J2, J5, J6,K2, K5, K6,L2, L3, L5,L6, M1, M2, N1, N2, N4,N5, N6, N7,P1, P3, P4,P7, P8	AGND	输入	模拟地
A9, B9, C9,D9, E9, F9,G9	DVDD09	输入	0.95V 数字内核电源
K10	DVDD18	输入	1.8V 数字接口电源
A10, B10, C10, D10, E10,F10, J8, G10, L10	DGND	输入	数字地
H8	RESET_ANALOG	输入	模拟电路复位管脚。一旦提供了主时钟，该管脚对时钟产生器进行复位。高电平时复位，正常工作时保持低电平，1.8V 逻辑。
H9	RESET_LOGIC	输入	数字电路复位管脚。高电平时复位，正常工作时请保持低电平。芯片上电时，芯片内部的 POR 电路会复位所有的数字电路，此时该复位信号可以忽略，1.8V 逻辑。
L8, K8	FD<0> FD<1>	输出	FD<0> 对应 I-channel，FD<1> 对应 Q 信号饱和快速检测管脚，channel，1.8V 逻辑。
M11, K11, K9, J10, J11	GPIO<4:0>	输入	用于 DDC 的快速频率跳转。1.8V 逻辑。
J9	TSKEW_BG	输入	该管脚为高电平时可以启动后台时序偏差校准（background timing skew calibration），1.8V 逻辑。
L9	SYNCB	输入	JESD204B 同步信号。低电平时，JESD204B 与接收器正进行握手，握手完成后，该管脚转为高电平，1.8V 逻辑。
P10	SPI_CSH	输入	SPI 片选使能信号，当 SPI 进行读写时，保持为 1，0 将复位 SPI，1.8V 逻辑。
N10	SCLK	输入	SPI 时钟信号，1.8V 逻辑。
M9	SPI	输入	SPI 输入信号，1.8V 逻辑。
M10	SDO	输出	SPI 输出信号，1.8V 逻辑。
P9	POWERDOWN	输入	芯片断电模式管脚，输入高电平将芯片断电，正常工作时保持低电平，1.8V 逻辑。
D11, H10, L11	NC	/	悬空，不连接。NC 引脚禁止接地或接高电平处理。
C12, D12, E12, G12, H12, J12, K12, L12, M12	JVDD09	输入	0.95V JESD204B 内核供电
F12	JVDD18	输入	1.8V JESD204B 接口 I/O 供电
A13, A14, C11, E11, F11, G11, H11, P13, P14	JGND	输入	JESD204B 接口地
N11	SERDOUT0_P	输出	Lane 0 差分 SerDes 输出对，内接 100 欧姆电阻
N12	SERDOUT0_N		
P11	SERDOUT1_P	输出	Lane 1 差分 SerDes 输出对，内接 100 欧姆电阻
P12	SERDOUT1_N		
N13	SERDOUT2_P	输出	Lane 2 差分 SerDes 输出对，内接 100 欧姆电阻
M13	SERDOUT2_N		
N14	SERDOUT3_P	输出	Lane 3 差分 SerDes 输出对，内接 100 欧姆电阻
M14	SERDOUT3_N		
L13	SERDOUT4_P	输出	Lane 4 差分 SerDes 输出对，内接 100 欧姆电阻
K13	SERDOUT4_N		
L14	SERDOUT5_P	输出	Lane 5 差分 SerDes 输出对，内接 100 欧姆电阻
K14	SERDOUT5_N		

管脚序号	管脚名	类型	功能描述
J13	SERDOUT6_P	输出	Lane 6 差分 SerDes 输出对, 内接 100 欧姆电阻
H13	SERDOUT6_N		
J14	SERDOUT7_P	输出	Lane 7 差分 SerDes 输出对, 内接 100 欧姆电阻
H14	SERDOUT7_N		
F14	SERDOUT8_P	输出	Lane 8 差分 SerDes 输出对, 内接 100 欧姆电阻
G14	SERDOUT8_N		
F13	SERDOUT9_P	输出	Lane 9 差分 SerDes 输出对, 内接 100 欧姆电阻
G13	SERDOUT9_N		
D14	SERDOUT10_P	输出	Lane 10 差分 SerDes 输出对, 内接 100 欧姆电阻
E14	SERDOUT10_N		
D13	SERDOUT11_P	输出	Lane 11 差分 SerDes 输出对, 内接 100 欧姆电阻
E13	SERDOUT11_N		
B14	SERDOUT12_P	输出	Lane 12 差分 SerDes 输出对, 内接 100 欧姆电阻
C14	SERDOUT12_N		
B13	SERDOUT13_P	输出	Lane 13 差分 SerDes 输出对, 内接 100 欧姆电阻
C13	SERDOUT13_N		
A11	SERDOUT14_P	输出	Lane 14 差分 SerDes 输出对, 内接 100 欧姆电阻
A12	SERDOUT14_N		
B11	SERDOUT15_P	输出	Lane 15 差分 SerDes 输出对, 内接 100 欧姆电阻
B12	SERDOUT15_N		

7. 技术规格（Specifications）

7.1. 电气特性（Electrical Characteristics）

表 3 电气特性

Parameter	Conditions	CYD2500			Unit
		Min	Typ	Max	
Analog Input					
Full-scale input range	Fully differential	0.5	0.8	1.0	Vpp,diff
Input Termination	Single-channel, differential		50		Ω
	Dual-Channel, differential		100		Ω
Single-ended Input capacitance	Single-ended to AGND		400		fF
Differential Input capacitance	Differential inputs		80		fF
Input Common Mode	VCM,input	0.40	0.45	0.50	V
Input Signal Bandwidth	-3dB bandwidth		3.0		GHz
SerDes Output					
Differential Output Voltage	Normal mode	0.45		0.50	Vpp,diff
Output Common Mode Voltage	AC coupled	0.57	0.63	0.79	V
Output Termination	Differential		100		Ω
Clock Input					
Differential Input Voltage	100 ohm differential, on-chip	0.3	1	2	Vpp,diff
Input Common Mode Voltage	VCM,CLKIN	0.2	0.3	0.4	V
Clock Frequency	FCLK			2.0	GHz
Duty Cycle			50.0		%
Single-ended Input Capacitance	Single-ended to AGND		400		fF
Differential Input Capacitance	Differential inputs		80		fF
SYSREF Input					
Differential Input Voltage	100 ohm differential, on-chip	0.5	1.0	2.0	Vpp,diff
Input Common Mode Voltage	VCM,SYSREFIN		0.9		V
Frequency	Periodic mode		12.5	31.25	MHz
Pulse Width	Burst and Periodic modes	500			ps
Singled-ended Input Capacitance	Single-ended to AGND		450		fF
Differential Input Capacitance	Differential inputs		90		fF
Reference Voltage					
Internal Reference Voltage	Fully Differential	±0.39	±0.4	±0.41	V
Tempco	From -40°C to 125°C		±50	±100	ppm/°C
DC Accuracy					
Resolution	DC code		12		bit
INL	Best-Fit		±1.3		LSB
DNL	(no missing code)		±0.4		LSB
Offset Error	DC code error		±3		Error/ mV
Code Error Rate	Whole chip		$< 10^{-15}$		samples
	Single-ChannelMode , 4 GSPS	Min	Typ	Max	
AC Accuracy					
	Fin = 180MHz, -1.0 dBFS (0.8Vpp FS)		52.1		dBFS
	Fin = 180MHz, -3.0 dBFS (0.8Vpp FS)		52.1		
	Fin = 180MHz, -1.0 dBFS (1.0Vpp FS)		53.6		dBFS
	Fin = 180MHz, -3.0 dBFS (1.0Vpp FS)		53.5		
	Fin = 1.09GHz, -1.0 dBFS (0.8Vpp FS)		51.5		dBFS
	Fin = 1.09GHz, -3.0 dBFS (0.8Vpp FS)		51.7		

Parameter	Conditions	CYD2500			Unit
		Min	Typ	Max	
SNR	Fin = 1.09GHz, -1.0 dBFS (1.0Vpp FS)		52.8		dBFS
	Fin = 1.09GHz, -3.0 dBFS (1.0Vpp FS)		53.1		
	Fin = 1.98GHz, -1.0 dBFS (0.8Vpp FS)		50.4		dBFS
	Fin = 1.98GHz, -3.0 dBFS (0.8Vpp FS)		51.0		
	Fin = 1.98GHz, -1.0 dBFS (1.0Vpp FS)		51.4		dBFS
	Fin = 1.98GHz, -3.0 dBFS (1.0Vpp FS)		52.1		
	Fin = 180MHz, -1.0 dBFS (0.8Vpp FS)		52.1		dBFS
	Fin = 180MHz, -3.0 dBFS (0.8Vpp FS)		52.1		
	Fin = 180MHz, -1.0 dBFS (1.0Vpp FS)		53.5		dBFS
	Fin = 180MHz, -3.0 dBFS (1.0Vpp FS)		53.5		
	Fin = 1.09GHz, -1.0 dBFS (0.8Vpp FS)		51.4		dBFS
	Fin = 1.09GHz, -3.0 dBFS (0.8Vpp FS)		51.7		
SINAD	Fin = 1.09GHz, -1.0 dBFS (1.0Vpp FS)		52.7		dBFS
	Fin = 1.09GHz, -3.0 dBFS (1.0Vpp FS)		53.1		
	Fin = 1.98GHz, -1.0 dBFS (0.8Vpp FS)		50.4		dBFS
	Fin = 1.98GHz, -3.0 dBFS (0.8Vpp FS)		50.9		
	Fin = 1.98GHz, -1.0 dBFS (1.0Vpp FS)		51.3		dBFS
	Fin = 1.98GHz, -3.0 dBFS (1.0Vpp FS)		52.0		
	Fin = 180MHz, -1.0 dBFS (0.8Vpp FS)		75.8		dBFS
	Fin = 180MHz, -3.0 dBFS (0.8Vpp FS)		76.4		
	Fin = 180MHz, -1.0 dBFS (1.0Vpp FS)		74.4		dBFS
	Fin = 180MHz, -3.0 dBFS (1.0Vpp FS)		72.2		
	Fin = 1.09GHz, -1.0 dBFS (0.8Vpp FS)		71.0		dBFS
	Fin = 1.09GHz, -3.0 dBFS (0.8Vpp FS)		72.0		
SFDR	Fin = 1.09GHz, -1.0 dBFS (1.0Vpp FS)		69.9		dBFS
	Fin = 1.09GHz, -3.0 dBFS (1.0Vpp FS)		75.5		
	Fin = 1.98GHz, -1.0 dBFS (0.8Vpp FS)		69.0		dBFS
	Fin = 1.98GHz, -3.0 dBFS (0.8Vpp FS)		70.8		
	Fin = 1.98GHz, -1.0 dBFS (1.0Vpp FS)		68.6		dBFS
	Fin = 1.98GHz, -3.0 dBFS (1.0Vpp FS)		70.5		
	Single-ChannelMode , 4 GSPS	Min	Typ	Max	
AC Accuracy					
	Fin = 180MHz, -1.0 dBFS (0.8Vpp FS)		-83.4		dBFS
	Fin = 180MHz, -3.0 dBFS (0.8Vpp FS)		-92.5		
	Fin = 180MHz, -1.0 dBFS (1.0Vpp FS)		-85.8		dBFS
	Fin = 180MHz, -3.0 dBFS (1.0Vpp FS)		-90.7		
	Fin = 1.09GHz, -1.0 dBFS (0.8Vpp FS)		-78.5		dBFS
	Fin = 1.09GHz, -3.0 dBFS (0.8Vpp FS)		-80.7		
HD2	Fin = 1.09GHz, -1.0 dBFS (1.0Vpp FS)		-76.6		dBFS
	Fin = 1.09GHz, -3.0 dBFS (1.0Vpp FS)		-79.3		
	Fin = 1.98GHz, -1.0 dBFS (0.8Vpp FS)		-90.3		dBFS
	Fin = 1.98GHz, -3.0 dBFS (0.8Vpp FS)		-89.8		
	Fin = 1.98GHz, -1.0 dBFS (1.0Vpp FS)		-96.9		dBFS
	Fin = 1.98GHz, -3.0 dBFS (1.0Vpp FS)		-89.8		
	Fin = 180MHz, -1.0 dBFS (0.8Vpp FS)		-77.6		dBFS
	Fin = 180MHz, -3.0 dBFS (0.8Vpp FS)		-79.4		
	Fin = 180MHz, -1.0 dBFS (1.0Vpp FS)		-74.4		dBFS
	Fin = 180MHz, -3.0 dBFS (1.0Vpp FS)		-76.7		
	Fin = 1.09GHz, -1.0 dBFS (0.8Vpp FS)		-72.1		dBFS
	Fin = 1.09GHz, -3.0 dBFS (0.8Vpp FS)		-79.3		

Parameter	Conditions	CYD2500			Unit
		Min	Typ	Max	
HD3	Fin = 1.09GHz, -1.0 dBFS (1.0Vpp FS)		-69.9		dBFS
	Fin = 1.09GHz, -3.0 dBFS (1.0Vpp FS)		-78.5		
	Fin = 1.98GHz, -1.0 dBFS (0.8Vpp FS)		-78.3		dBFS
	Fin = 1.98GHz, -3.0 dBFS (0.8Vpp FS)		-73.9		
	Fin = 1.98GHz, -1.0 dBFS (1.0Vpp FS)		-75.2		dBFS
	Fin = 1.98GHz, -3.0 dBFS (1.0Vpp FS)		-74.3		
	Fin = 180MHz, -1.0 dBFS (0.8Vpp FS)		8.4		Bit
	Fin = 180MHz, -3.0 dBFS (0.8Vpp FS)		8.4		
	Fin = 180MHz, -1.0 dBFS (1.0Vpp FS)		8.6		Bit
	Fin = 180MHz, -3.0 dBFS (1.0Vpp FS)		8.6		
	Fin = 1.09GHz, -1.0 dBFS (0.8Vpp FS)		8.3		Bit
	Fin = 1.09GHz, -3.0 dBFS (0.8Vpp FS)		8.3		
ENOB	Fin = 1.09GHz, -1.0 dBFS (1.0Vpp FS)		8.5		Bit
	Fin = 1.09GHz, -3.0 dBFS (1.0Vpp FS)		8.5		
	Fin = 1.98GHz, -1.0 dBFS (0.8Vpp FS)		8.1		Bit
	Fin = 1.98GHz, -3.0 dBFS (0.8Vpp FS)		8.2		
	Fin = 1.98GHz, -1.0 dBFS (1.0Vpp FS)		8.2		Bit
	Fin = 1.98GHz, -3.0 dBFS (1.0Vpp FS)		8.4		
AC Accuracy					
Noise Floor Density	At 180MHz, -1 dBFS (1Vpp FS)		-146.6		dBFS/√Hz
Speed					
ADC Sampling rate	Single-channel		4		GSPS
	Dual-Channel		2		GSPS
JESD204B lane rate	SerDes lane rate, 100 ohm termination	1.6875	5	10	Gbps
Power Supplies					
AVDD18,DVDD18,JVDD18	1.8V power supplies	1.7	1.8	1.9	V
DVDD09,JVDD09	0.95V power supplies	0.9	0.95	0.975	V
BVNN08	Analog negative power supplies Normal mode, all background	-0.95	-1.0	-1.05	V
Current (1.8V supplies)	calibrations enable & DDC off Normal mode, all background		805		mA
Current (0.95V supplies)	calibrations enable & DDC off		550		mA
Current (1.8V supplies)	Power down		66		mA
Current (0.95V supplies)	Power down Normal mode, all background		11		mA
Power Consumption	calibrations enable & DDC off		2.0		W
Junction Temperature	TMIN to TMAX	-40		115	°C
Long-Term Reliability	For Pro-longed use	-40		105	°C

7.2. 时序要求（Timing Requirements）

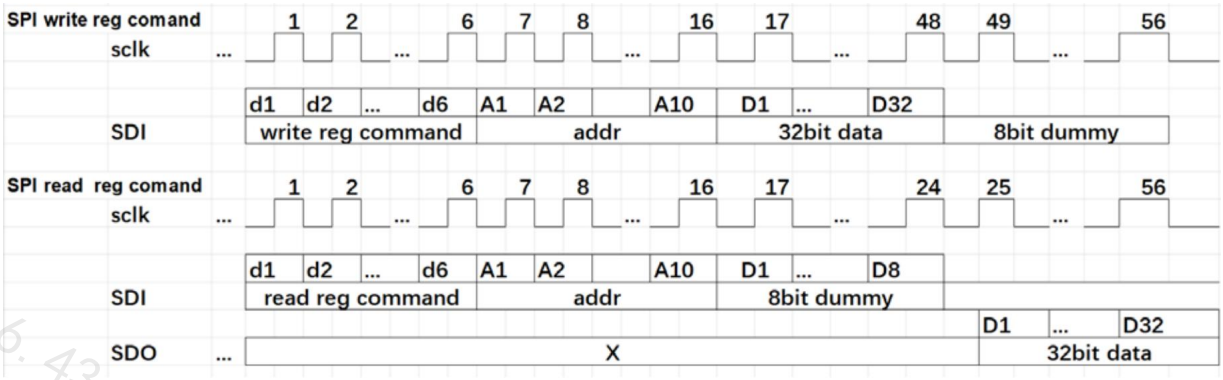

图 3 SPI 读写数据：接口波形

芯片复位后 SPI 读写寄存器，相关的信号 SPI_CSH 默认为 1。

SPI 读写寄存器需要 56bits。6 位命令字+ 10 位为地址+40 位数据。
6 位命令字的控制为 6b0001_00 写寄存器，6b0010_00 读寄存器。
其中地址 0x_xxxx_xxxx 为芯片 SPI 寄存器。1x_xxxx_xxxx 为 JESD204B APB 寄存器。

以 SPI 写 SPI 第一寄存器 32'h14183102 为例：spi_wr_reg(10'h001,32'h14183102) 测试 pattern 波形：前面 6 个 sclk，对应 SDI 为 6b0001_00，所以是 SPI 写。后面 10 个 SCLK，对应的是地址，数据为 00_0000_0001，表示写的是 001 寄存器。再接着的 32 个 SCLk，对应的数据是 14,18,31,02 表示写入 01 寄存器的数值为 32'h14183102. 最后的 8 个 sclk，对应的 SDI 为 0，是无用的数据。（SPI_CSH=1）

以 spi_rd_reg(10'h000,temp32b) 即读第 0 寄存器的结果为例，说明 SPI 读对应的波形：

前面 6 个 sclk，对应 SDI 为 6b0010_00，所以是 SPI 读命令。后面 10 个 SCLK，对应的是地址，数据为 00_0000_0000，表示读的是 SPI 000 寄存器。再接着的 8 个 sclk, 对应 SDI 数据为 0，为 8bits dummy，最后面的 32 个对应的 SDI 数据是 0，而此时对应的 SDO 的输出为读出结果。（SPI_CSH=1）

测试激励信号是下降沿给 SDI 数据，芯片内部是上升沿抓数。芯片给出的 SDO 信号是 SCLK 上升沿给出，仪器下降沿去抓 SDO 结果。

对 JESD204B APB 寄存器的读写：
读写 APB 寄存器需要 56bits。6 位命令字+ 10 位地址+ 40 位数据。6b0001_00 写 APB 寄存器，6b0010_00 读 APB 寄存器。
例：APB 写第四寄存器，数据为 80H，格式为 6'b0001_00 + 10'b10_0000_0100 + 8'h80+ 32'h0dummy。APB 读第四寄存器，6'b0010_00 + 10'b10_0000_0100 + 8bits dummy+ 8bits data + 24bits dummy。

7.3. 典型特性（Typical Characteristics）

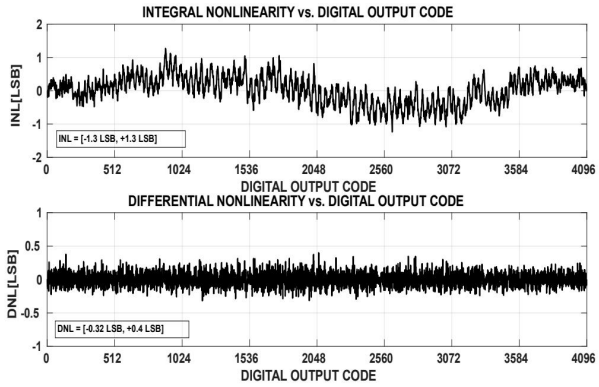

图 4 INL/DNL at Fin = 180MHz, 4GSPS(0.8VppFS)

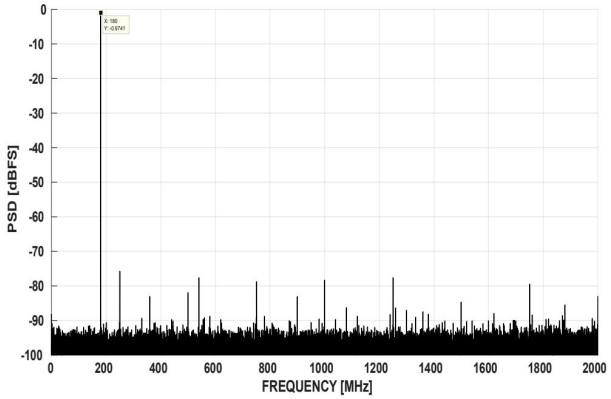

图 5 FFT at Fin = 180MHz, 4GSPS(0.8VppFS)

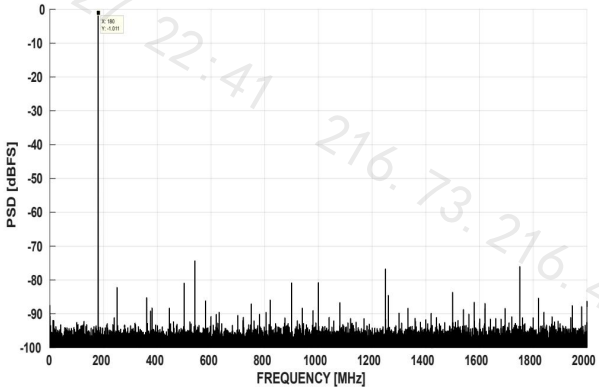

图 6 FFT at Fin = 180MHz, 4GSPS(1.0VppFS)

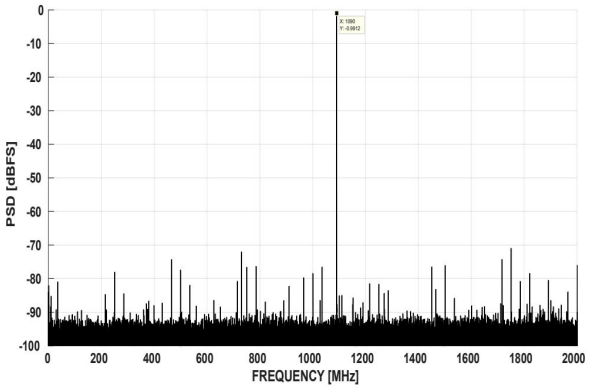

图 7 FFT at Fin = 1.09GHz, 4GSPS(0.8VppFS)

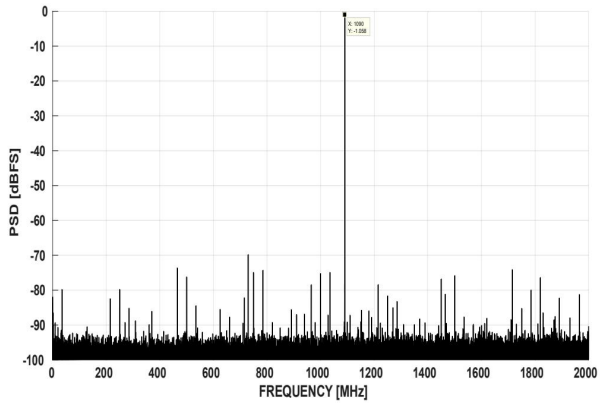

图 8 FFT at Fin = 1.09GHz, 4GSPS(1.0VppFS)

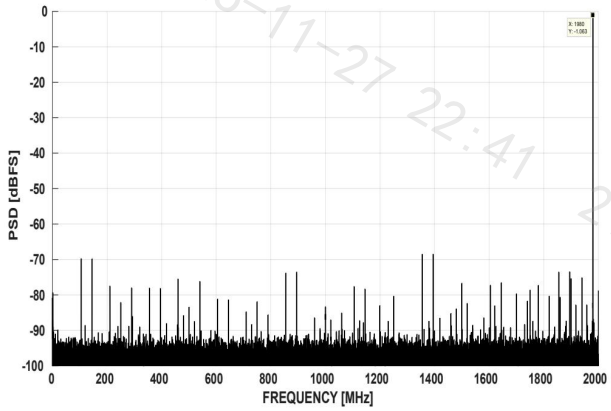

图 9 FFT at Fin = 1.98GHz, 4GSPS(1.0VppFS)

8. 详细说明（Detailed Description）

8.1. 概述（Overview）

CYD2500 是一款 12 位、高速射频采样模数转换器（ADC），单通道模式下的最大采样率为 4GSPS，双通道模式下的最大采样率为 2GSPS。单通道或者双通道工作模式可在线编程配置，可用于开发灵活的硬件，以满足高通道数或宽瞬时信号带宽应用的需求。CYD2500 采用高速 JESD204B 输出接口，工作温度（结温）支持 -40 to 115°C，使用 FCBGA196 (12mm x 12mm) 封装。

8.2. 功能框图（Functional Block Diagram）

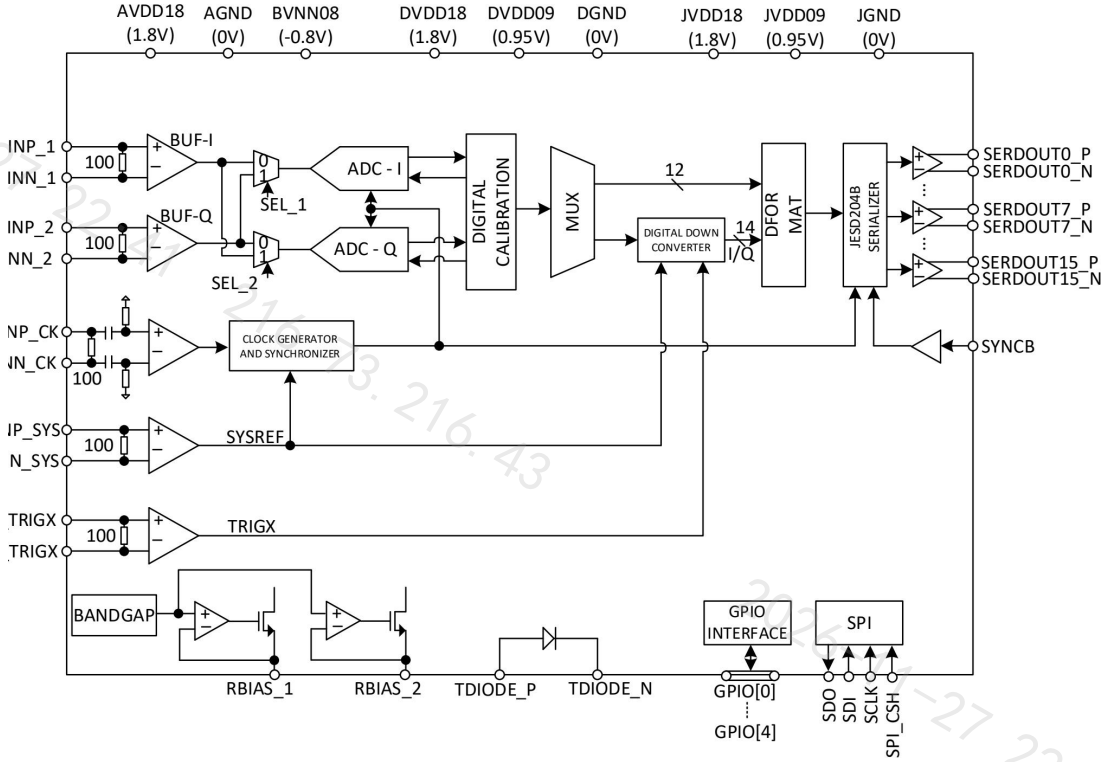

图 10 功能框图

8.3. 信号管脚连接说明

CYD2500 信号管脚按功能类型可分为以下 9 类：

表 4 信号管脚分类

类别序号	信号管脚类别	管脚数量	信号管脚名称
1	模拟信号输入管脚	4	AINP_1/ AINN_1 AINP_2/ AINN_2
2	主时钟输入管脚	2	AINP_CK/ AINN_CK
3	SYSREF 同步信号输入管脚	2	AINP_SYSREF/ AINN_ SYSREF
4	TRIGX 信号输入管脚	2	AINP_TRIGX/ AINN_ TRIGX
5	模拟参考偏置电流管脚	2	RBIAS<0> 、RBIAS<1>
6	温度二极管管脚	2	TDIODE_P / TDIODE_N
7	数字 IO 输入管脚(1.8V 电平)	13	RESET_ANALOG、RESET_LOGIC TSKEW_BG、GPIO<0> GPIO<1> 、GPIO<2> GPIO<3> 、GPIO<4> SDI、SCLK、SPI_CSH POWERDOWN、SYNCB
8	数字 IO 输出管脚(1.8V 电平)	3	FD<0> 、FD<1> 、SDO
9	JESD204B SerDes 高速输出管脚	32	SERDOUT0_P/ SERDOUT0_N SERDOUT1_P/SERDOUT1_N SERDOUT2_P/ SERDOUT2_N SERDOUT3_P/ SERDOUT3_N SERDOUT4_P/ SERDOUT4_N SERDOUT5_P/SERDOUT5_N SERDOUT6_P/ SERDOUT6_N SERDOUT7_P/ SERDOUT7_N SERDOUT8_P/ SERDOUT8_N SERDOUT9_P/ SERDOUT9_N SERDOUT10_P/ SERDOUT10_N SERDOUT11_P/ SERDOUT11_N SERDOUT12_P/ SERDOUT12_N SERDOUT13_P/SERDOUT13_N SERDOUT14_P /SERDOUT14_N SERDOUT15_P/ SERDOUT15_N

1.模拟信号输入管脚：AINP1 / AINN1、AINP2 / AINN2

模拟信号输入管脚支持交流（AC）耦合以及直流（DC）耦合两种连接方式。

其中 AINP_1/ AINN_1 为模拟输入通道 1 的差分输入端口，AINP_2/ AINN_2 为模拟输入通道 2 的差分输入端口。

每个模拟输入通道内建有 100 欧姆差分端接电阻。内部钳位二极管可防止输入信号功率过高导致模拟输入通道上器件被烧毁。

PCB 上连接至模拟信号输入管脚的走线需严格按照单端 50 欧姆/ 差分 100 欧姆做好阻抗控制，不合理的走线阻抗会导致模拟输入信号产生严重的反射。同时，模拟输入信号的 PCB 走线应尽量避免经过通孔，并做好隔离，防止其他信号线或者噪声较大的电源干扰。

为了减少 PCB 走线对模拟输入信号的损耗，PCB 板材尽可能选用高频/高速板材，例如 Rogers 的 RO4350B 或者松下的 M6 等。

交流（AC）耦合连接说明:

如图 11 所示，当交流（AC）耦合连接时，模拟信号输入管脚需外部提供 0.45V 差分输入共模电压（VCMI）。该 VCMI 电压可以通过外部电阻分压产生，并通过 2K 欧电阻连接至模拟信号输入管脚。

需要注意，两个模拟输入通道的 VCMI 必须各自独立。共用 VCMI 可能导致两个模拟通道之间相互干扰。

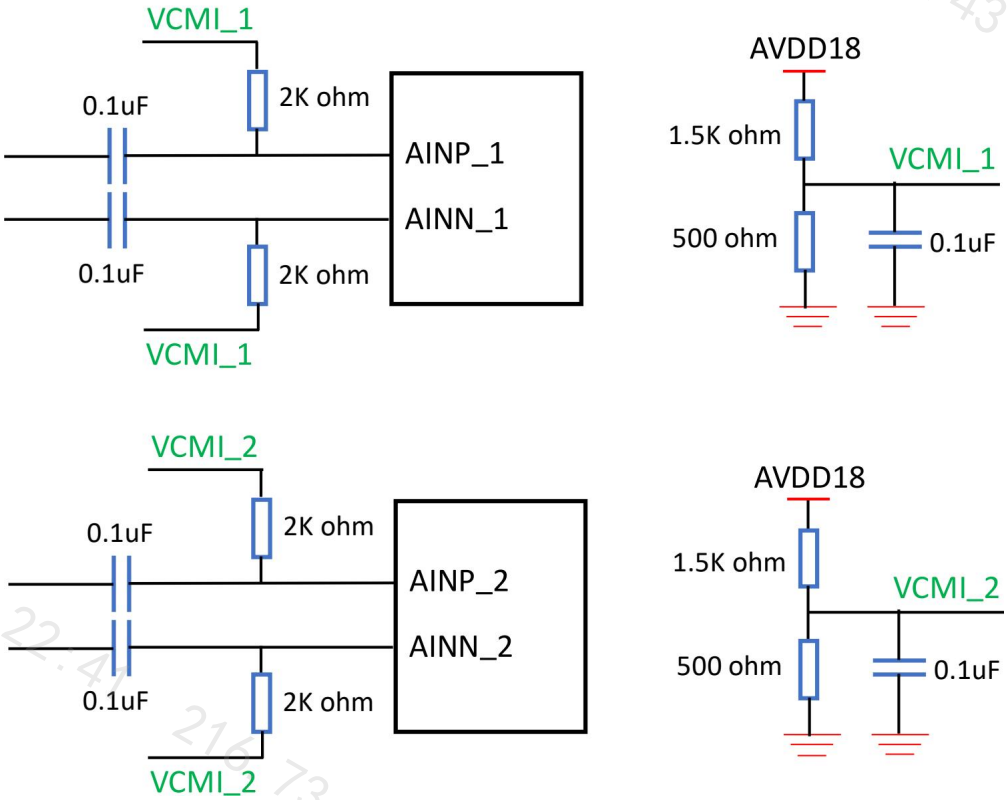

图 11 模拟信号输入管脚交流（AC）耦合连接示意图

直流（DC）耦合连接说明:

如图 12 所示，当直流（DC）耦合连接时，模拟信号输入管脚可以直连模拟前端的差分输出（例如差分运放输出），但该模拟前端的差分输出共模电压需为 0.45V。

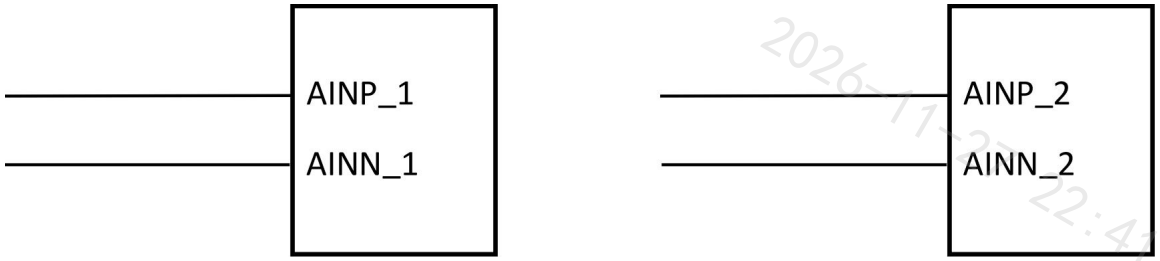

图 12 模拟信号输入管脚直流（DC）耦合连接示意图

2. 主时钟输入管脚：AINP_CK / AINN_CK

主时钟输入管脚 AINP_CK/ AINN_CK 仅支持交流（AC）耦合连接方式。

如图 13 所示，高频输入时钟通过 0.1uF 隔直电容，交流耦合至 AINP_CK/ AINN_CK。

为了最大化输入时钟的摆幅，主时钟输入管脚需外部提供差分共模电压（VCM_CLK），该 VCM_CLK 可以通过外部电阻分压产生，分压电源（VDD_CLK）需使用时钟电源或者单独的电源，避免使用 ADC 的 1.8V 模拟电源，以便减小时钟对模拟输入通路的干扰。

时钟通路内部有 100 欧姆端接电阻。

PCB 上连接至主时钟输入管脚的走线需严格按照单端 50 欧姆/ 差分 100 欧姆做好阻抗控制，不合理的走线阻抗会导致主时钟输入信号产生严重的反射。

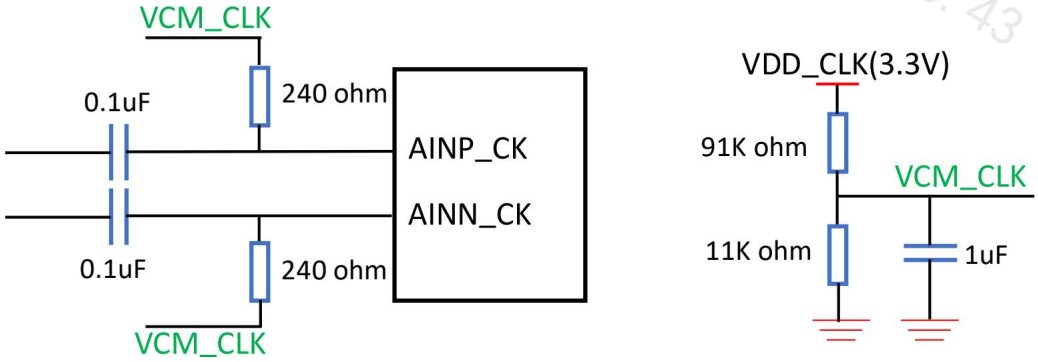

图 13 主时钟输入管脚交流（AC）耦合连接示意图

3. SYSREF 同步信号输入管脚：AINP_SYSREF / AINN_ SYSREF

SYSREF 同步信号输入管脚支持交流（AC）耦合以及直流（DC）耦合两种连接方式。

该差分输入管脚内部有 100 欧姆端接电阻，并且内部有共模电压产生电路，无需外部提供共模电压。

图 14 为该差分输入管脚的连接示意图。

PCB 上连接至 SYSREF 同步信号输入管脚的走线需严格按照单端 50 欧姆/ 差分 100 欧姆做好阻抗控制，不合理的走线阻抗会导致 SYSREF 同步信号输入信号产生严重的反射。该 SYSREF 同步信号需要有支持产生 SYSREF 信号的时钟芯片产生。

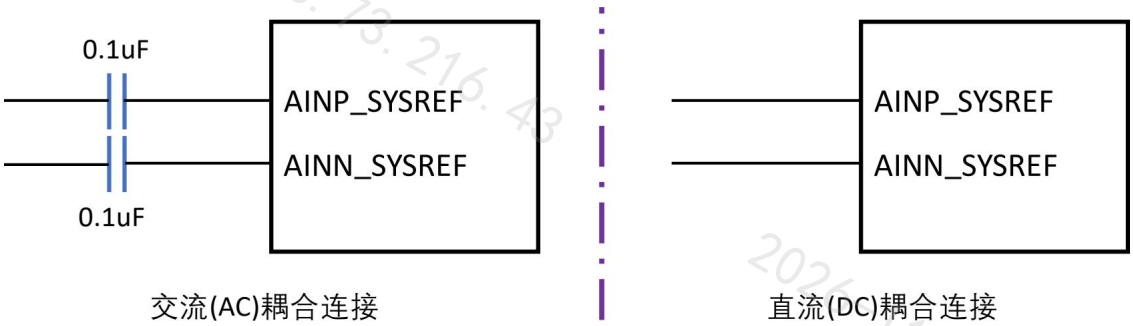

图 14 SYSREF 同步信号输入管脚交流（AC）耦合/ 直流（DC）耦合连接示意图

4. TRIGX 信号输入管脚：AINP_TRIGX / AINN_ TRIGX

TRIGX 信号输入管脚支持交流（AC）耦合以及直流（DC）耦合两种连接方式。

该差分输入管脚内部有 100 欧姆端接电阻，并且内部有共模电压产生电路，无需外部提供共模电压。

图 15 为该差分输入管脚的连接示意图。

PCB 上连接至 TRIGX 信号输入管脚的走线需严格按照单端 50 欧姆/ 差分 100 欧姆做好阻抗控制，不合理的走线阻抗会导致 TRIGX 信号输入信号产生严重的反射。

该 TRIGX 信号可以通过 FPGA 的差分输出 IO 产生。

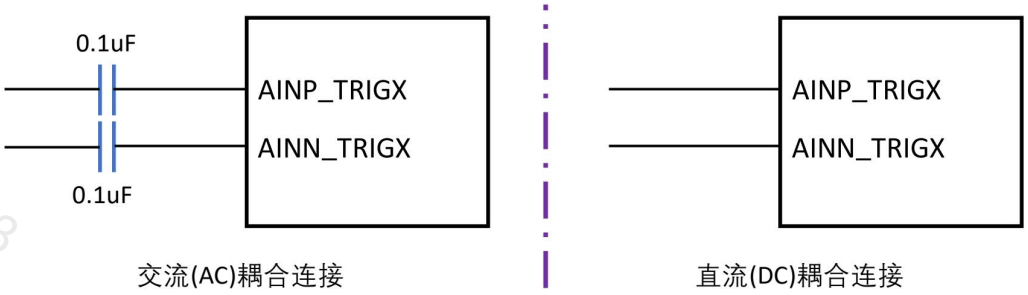

图 15 TRIGX 信号输入管脚交流（AC）耦合/ 直流（DC）耦合连接示意图

5. 模拟参考偏置电流管脚：RBIAS<0>、RBIAS<1>

RBIAS<0>、RBIAS<1>用于产生模拟电路内部精准参考偏置电流。

如图 16 所示，每个管脚各通过一个 12K 欧姆电阻接地。

该 12K 电阻的精度需要小于或等于 1%（0.1%精度更佳），同时电阻温度系数需要小于或等于 25ppm。

12K 电阻推荐使用 0402 或者 0201 封装。

PCB 上该 12K 电阻需尽量靠近芯片管脚放置，以减小走线长度。同时做好隔离，避免噪声信号或者电源干扰。

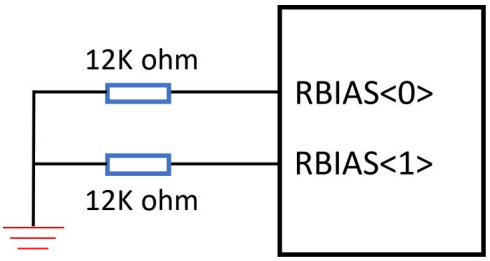

图 16 模拟参考偏置电流管脚 RBIAS<0>、RBIAS<1>连接示意图

6. 温度二极管管脚：TDIODE_P / TDIODE_N

TDIODE_P / TDIODE_N 为 CYD2500 芯片内部温度二极管管脚。如图 17 所示，该管脚可连接至外部测温芯片，以实时监控 CYD2500 内部结温，防止芯片内部过热导致性能下降或者老化。图中串联电阻 Rs 以及差分电容 Cdiff 的数值需要根据实际所选的测温芯片的要求决定。

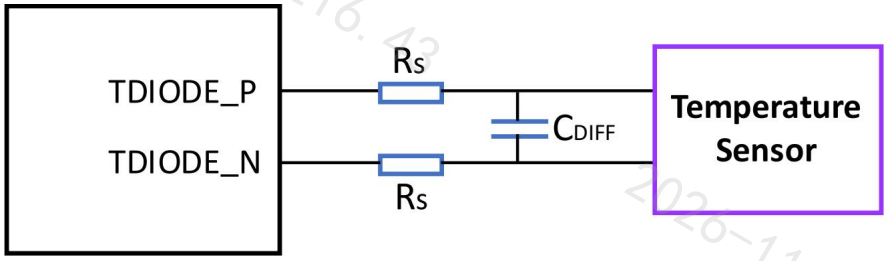

图 17 温度二极管管脚 TDIODE_P / TDIODE_N 连接示意图

7.数字 IO 输入管脚（1.8V 电平）：RESET_ANALOG、RESET_LOGIC、TSKEW_BG、GPIO<0>、GPIO<1>、GPIO<2>、GPIO<3>、GPIO<4>、SDI、SCLK、SPI_CSH、POWERDOWN、SYNCB

CYD2500 一共有 13 个数字 IO 输入管脚。每个管脚的具体功能请参考表 2。

目前 5 个 GPIO 引脚仅支持输入功能，不支持输出。

如图 18 所示，13 个数字 IO 输入管脚通过可选的 0 欧姆电阻连接至 FPGA 的 1.8V 电平 IO 管脚。

如果 FPGA 的 IO 管脚不是 1.8V 电平，则需通过外部电平转换芯片转换成 1.8V 电平的 IO，再连接至 CYD2500 的数字 IO 管脚。

RESET_ANALOG 以及 RESET_LOGIC 管脚，可以在 PCB 上增加复位按钮电路（下图红色虚线框），通过板载按钮开关实现硬件快速复位。

不使用的数字 IO 输入管脚需要接地或者接 1.8V 高电平处理，避免悬空。

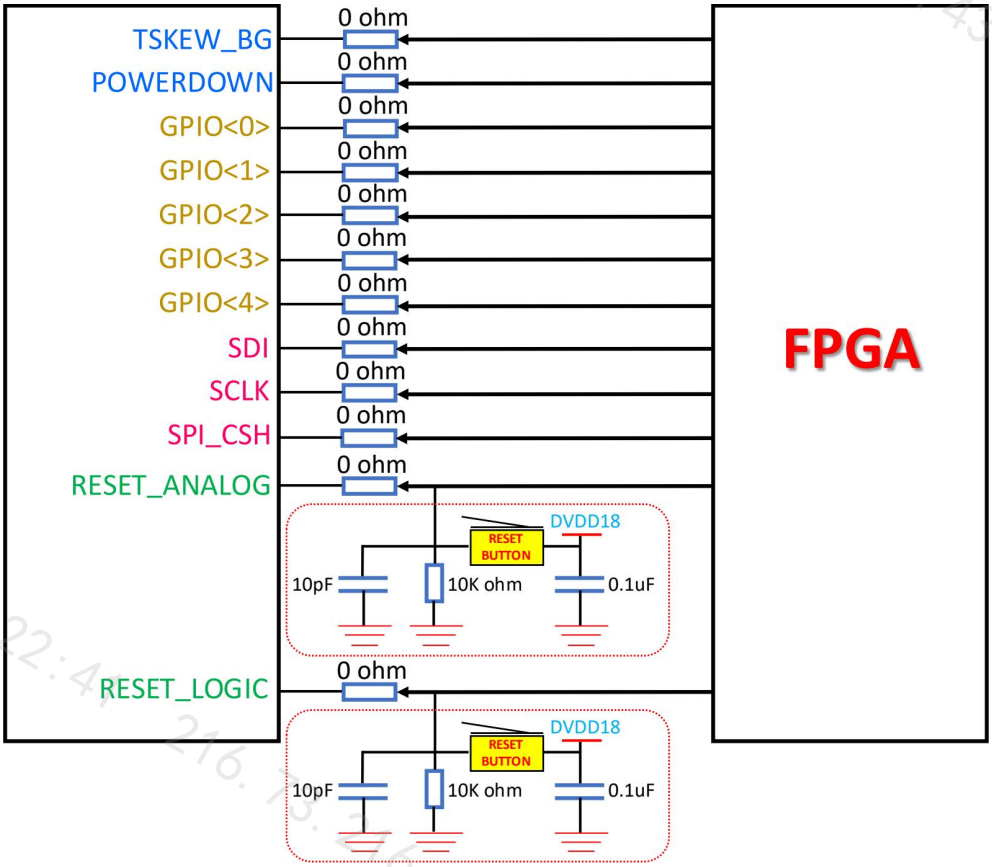

图 18 数字 IO 输入管脚（1.8V 电平）连接示意图

8. 数字 IO 输出管脚（1.8V 电平）：FD<0>、FD<1>、SDO

CYD2500 一共有 3 个数字 IO 输出管脚。每个管脚的具体功能请参考表 2。

如图 19 所示，3 个数字 IO 输出管脚通过可选的 0 欧姆电阻连接至 FPGA 的 1.8V 电平 IO 管脚。

如果 FPGA 的 IO 管脚不是 1.8V 电平，则需通过外部电平转换芯片转换成 1.8V 电平的 IO。

不使用的数字 IO 输出管脚可以悬空。但不能直接接地或者接高电位。

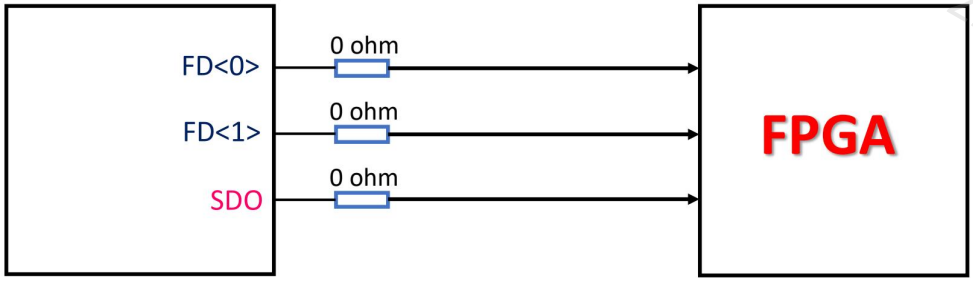

图 19 数字 IO 输出管脚（1.8V 电平）连接示意图

9. JESD204B SerDes 高速输出管脚：

SERDOUT0_P / SERDOUT0_N、SERDOUT1_P / SERDOUT1_N、SERDOUT2_P / SERDOUT2_N

SERDOUT3_P / SERDOUT3_N、SERDOUT4_P / SERDOUT4_N、SERDOUT5_P / SERDOUT5_N

SERDOUT6_P / SERDOUT6_N、SERDOUT7_P / SERDOUT7_N、SERDOUT8_P / SERDOUT8_N

SERDOUT9_P / SERDOUT9_N、SERDOUT10_P / SERDOUT10_N、SERDOUT11_P / SERDOUT11_N

SERDOUT12_P / SERDOUT12_N、SERDOUT13_P / SERDOUT13_N、SERDOUT14_P / SERDOUT14_N

SERDOUT15_P / SERDOUT15_N

CYD2500 一共有 16 lane JESD204B SerDes 高速输出管脚。

如图 20 所示，每个管脚通过 0.1uF 隔直电容交流耦合连接至 FPGA 的 RX 高速收发器。

PCB 上 16 lane SerDes 走线需严格按照单端 50 欧姆/差分 100 欧姆做好阻抗控制。并且 16 lane 之间需做等长处理。SerDes 的 lane 与 lane 之间需保证有不低于-33dB 的隔离度。

为减少 SerDes 信号的走线损耗，PCB 板材需要选用高频/高速板材，例如 Rogers 的 RO4350B 或者松下的 M6 等。

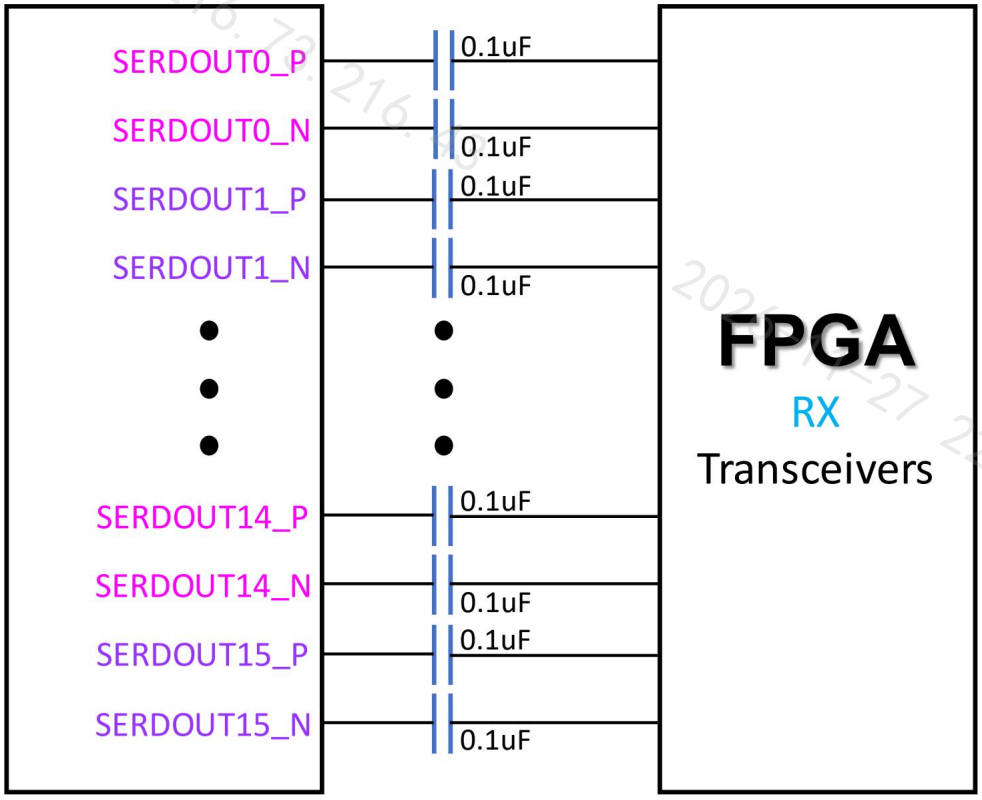

图 20 JESD204B SerDes 高速输出管脚连接示意图

8.4. 电源连接说明

CYD2500 有 3 组 1.8V 电源，2 组 0.95V 电源，2 组-1V 负电源。

图 21 是 CYD2500 电源连接的方案的示意图。

图中由 12V 电源适配器连接到 3 个 DCDC，再通过 4 个 LDO 产生 6 路电源给到 CYD2500。

其中 AVDD18 为 CYD2500 模拟电路电源，需要由单独的 LDO 供电以减少噪声干扰。

DVDD18 与 JVDD18 可以共用一个 LDO，但是需要通过磁珠（Ferrite Bead）或者馈通电容滤波器（Feed through filter）分离这两路电源。

DVDD09 与 JVDD09 可以共用一个 LDO，但是需要通过磁珠（Ferrite Bead）或者馈通电容滤波器（Feed through filter）分离这两路电源。如果选用的 LDO 无法提供 4A 或以上电流，则这两路电源可能需要分开由各自的 LDO 供电。

BVNN08<0>与 BVNN08<1>需要在 PCB 上连接到一起，并由同一路负电源供电。分开供电可能导致两路负电源出现电位差，从而影响性能。

PCB 上电源层的电流密度应不低于图中的推荐值，并尽可能留有余量，确保电源层寄生电阻小。

上电顺序需要保证 1.8V 电源先于 0.95V 电源上电。如果 0.95V 电源先上电，可能导致数字 IO 管脚出现漏电。尽量避免出现只有 0.95V 电源上电但是 1.8V 电源没有上电的情况，数字 IO 持续性的漏电可能导致芯片出现不可逆的损坏。

AGND、DGND、JGND 三个地需要在 PCB 上短接在一起。

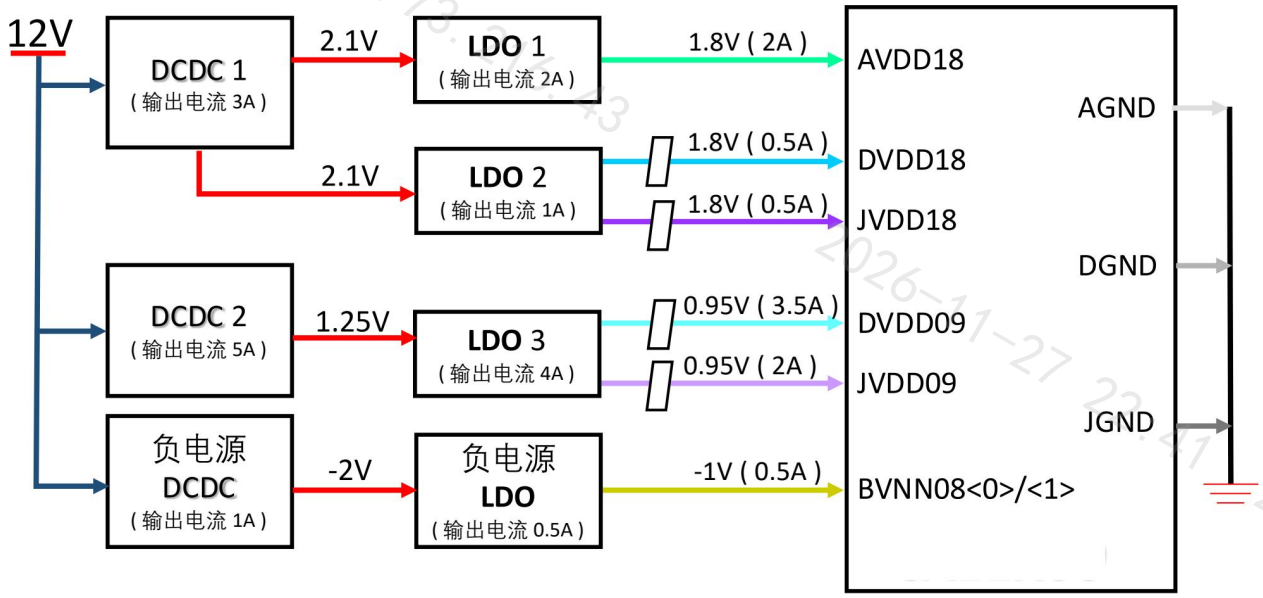

图 21 推荐电源连接示意图

（图中 DCDC 到 LDO 的输出电压值仅为参考，具体电压值需要根据实际使用的 DCDC 器件以及 LDO 器件决定）

8.5. 电源滤波电容放置说明

CYD2500 各组电源在 PCB 上需要就近放置滤波电容以减小电源波动对 ADC 性能的影响。

图 22 是 CYD2500 电源管脚滤波电容就近放置的参考示意图图中默认 PCB 采用树脂塞孔工艺且滤波电容封装尺寸为 0201，此时滤波电容可以放置在 PCB 背面 CYD2500 的电源管脚与 GND 管脚位置，。

需要注意的是图中 NC 管脚与 JVDD09 管脚位置的电容仅表示当 NC 管脚为悬空状态且焊盘上没有通孔 PCB 背面 NC 管脚下方实际是 GND 时，该位置可以放置个 0201 封装的滤波电容。将 NC 管脚接地或者用电容连接 NC 管脚与 JVDD09 电源管脚都可能导致 ADC 芯片无法工作。

图中 AVDD18 的电容位置为 PCB 上建议预留的电容焊盘位实际表贴的电容数量可以根据具体的电源以及布线情况调整。如果电容位置不是全部表贴上电容的话，则表贴的电容需要尽可能交错均匀放置，尽量避免只在某一边或者某几个电源管脚上放置电容。

DVDD18 以及 JVDD18 电源建议在靠近 ADC 芯片附近增加到两个电容位。

滤波电容建议使用个 1uF 配多个 01uF 的组合以便减少电源的低频高频噪声。

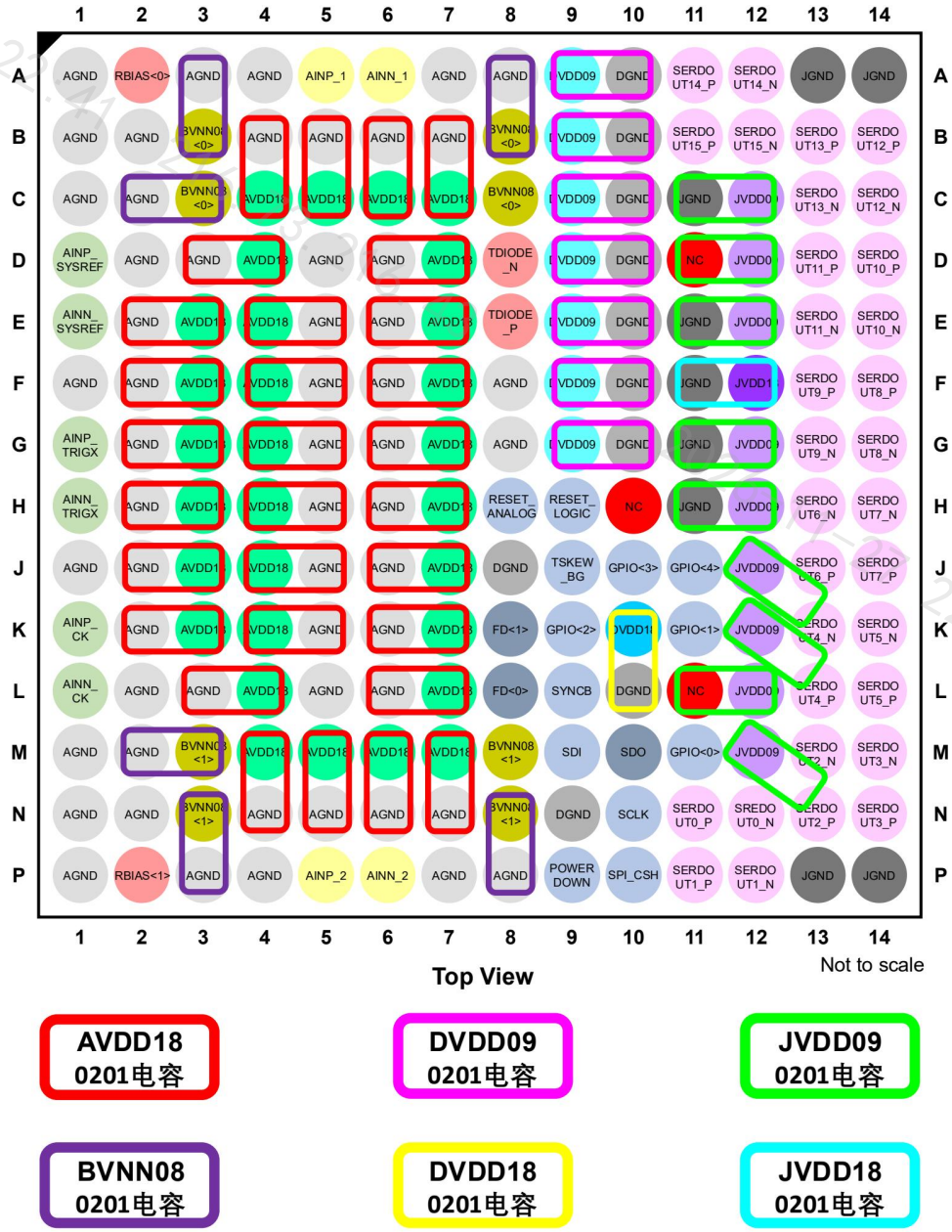

图 22 推荐各电源滤波电容放置参考示意图

8.6. 寄存器说明（Memory Map）

控制寄存器（地址 9h05 32’ h0042_9648）

表 5 控制寄存器位定义

Bits	Name	Default	Descriptions
31	bg_always	1’b0	Background timing skew always do
30	bg_fpga	1’b0	When 1,reg03 FPGA rr write is update to tskew module;0 not update
29	tskew_hd_en	1’b0	Tskew_bg_pin is enable to control background timing skew
28:27	Uf_range	2’h0	Ultra_fine ok range. 1,2,3or 4
26:24	bgpd_mode	3’h0	Background timing skew power down timing set(see below table)
23	Ufwin_en	1’b0	Ultra_fine_detect window function enable
		’	000: 1;001 div2;010 div4;011div8,100div16 : timing skew matrix
22:20	tsrx_th	3b100	reuslt/N for rr
19	tsfir_en	1’b0	1:Timing skew input FIR enable;default 0 : disable
18	Dual_mode	1’b0	default0: 16ch; 1 dual 8ch
17	fg_mode_spi	1’b1	force finecap msb result=1
16	sel_otp_data	1’b0	Timing skew mode1/2 start from otp value (avoid many time to get better result)
15:14	bg_thres	2’b10	background timing skew threshold
13:12	bg_mode	2’b01	background timing skew mode
11:8	tskew_mode	4’b0110	Timing skew discard/average samples setting
7	inv_ts_mode	1’b0	Timing skew sgn result inverse
6:4	bg_ts_mode	3’b100	Background timing skew loop number
3:2	bg_repeat	2’b10	M_threshold for +/- as one big loop
1	tskew_bg	1’b0	Background timing skew enable
0	tskew_fg	1’b0	Foreground timing skew enable

控制寄存器（地址 8h06 32’ h4000_7958）

表 6 控制寄存器位定义（续）

Bits	Name	Default	Descriptions
31:8	RVD		
7	p2SnOf	1’b1	code16 output 2's code(default) or offset code
6:0	RVD		

DDC 控制寄存器(地址 9h1C 32’ h0010_0000)

表 7 DDC 控制寄存器位定义

Bits	Name	Default	Descriptions
31:0	PST	32’h0010_0000	profile timer number

DDC 控制寄存器(地址 9h08 32’ h0301_0000)

表 8 DDC 控制寄存器位定义（续）

Bits	Name	Default	Descriptions
31:27	RVD		
26:24	{{sync_en,sync_next,	3’b011	Register setting description SYSREF_x edge used to synchronize the PAWs 100 all subsequent edges for SYSREF_xsignal reset all the PAWs in the chip 110 the next valid edge of SYSREF_x signal reset all the PAWs in
	trig_rst_en}}		the chip 001 all edges of SYSREF_x signal after TRIGGER signal reset all the PAWs in the chip 011 the next valid edge of SYSREF_x signal after TRIGGER signal reset all the PAWs in the chip
23:20	nco_nu_mode	4’h0	Nco number mode.0:NCO from reg;1 NCO from edge;2: NCO from GPIO; 3: NCO from profile select timer
19:18	reg_nu	2’b00	Nco number from register : choose one of 4NCO
17	Trig_spi	1’b0	SPI trig enable command
16	PD_TRIG	1’b1	1 power down trig ana,0 power on : default 1
15:8	Sysref_delay	8’h00	Sysref input delay
7:0	Trig_delay	8’h00	Trig input delay

DDC 控制寄存器(地址 8h09 32’ h8001_4000)

表 9 DDC 控制寄存器位定义

Bits	Name	Default	Descriptions
31	ddc_soft_rstb	1’b1	Write 0 will reset ddc module
30:28	Uf_window	3’h0	Timing Ultra_fine window steady skew cap value.0:8;1:16;2:32;3:64;4:128;5:256;6:512;7:1024
27:25	RVD		
24	Mid_tskew	1’b0	middle 1:Background timing mode0 start from skew value1000_0000;0: current value
23:18	RVD		
17	Ddc_fs4	1’b0	1/4 Fs mode
16	ddc_zif	1’b0	NCO Zero IF , no need NCO and mixer
15:13	ddc_mac_mode	3’b100	DDC MA average number.0: 2^14, 1 2^15; 2 2^16 ... 6 2^20 ; 7 2^21
12	ddc_debug_mode	1’b0	1:DDC result MA from SPI; 0 from MA module
11	ddc_test_mode	1’b0	The input sampls are forces to positive full scale and the NCO is enabled. This test mode allows the NCOs to directly drive the decimation filters
10	ddc_gain_6db	1’b0	DDC gain 6DB
9	ddc_c2r_en	1’b0	DDC Complex to real enable
8	hb1_en	1’b0	DDC Hb1 FIR enable
7	tb2_en	1’b0	DDC Tb2 FIR enable
6	hb2_en	1’b0	DDC Hb2 FIR enable
5	hb3_en	1’b0	DDC Hb3 FIR enable
4	hb4_en	1’b0	DDC Hb4 FIR enable
3	hb5_en	1’b0	DDC Hb5 FIR enable
2	hb6_en	1’b0	DDC Hb6 FIR enable
1	hb7_en	1’b0	DDC Hb7 FIR enable
0	ddcen	1’b0	DDC enable

DDC 控制寄存器 for PHASE: only 4 NCO support if 16ch mode, set phas0—phase3.
in dual_mode, phase4--phase7 for adc2

表 10 控制寄存器位定义

Bits	Name	Default	Descriptions
47:0	{reg168[15:0] ,reg160[31:0]}	48'd32056872347602	Phase0: 41 degree (41/360) * 2^48
47:0	{reg168[31:16],reg161[31:0]}	48'd32056872347602	Phase1: 41 degree (41/360) * 2^48
47:0	{reg169[15:0] ,reg162[31:0]}	48'd32056872347602	Phase2:41 degree (41/360) * 2^48
47:0	{reg169[31:16],reg163[31:0]}	48'd32056872347602	Phase3:41 degree (41/360) * 2^48
47:0	{reg16a[15:0] ,reg164[31:0]}	48'd30493122476988	Phase4:39 degree (39/360) * 2^48
47:0	{reg16a[31:16],reg165[31:0]}	48'd30493122476988	Phase5:39 degree (39/360) * 2^48
47:0	{reg16b[15:0] ,reg166[31:0]}	48'd30493122476988	Phase6:39 degree (39/360) * 2^48
47:0	{reg16b[31:16],reg167[31:0]}	48'd30493122476988	Phase7:39 degree (39/360) * 2^48

DDC 控制寄存器 for FTW only 4 NCO support if 16ch mode, set FTW0--FTW3.
in dual_mode, FTW4--FTW7 for adc2

表 11 控制寄存器位定义（续）

Bits	Name	Default	Descriptions
47:0	{reg150[15:0] ,reg16C[31:0]}	48'd136339441844233	FTW0:
47:0	{reg150[31:16],reg16D[31:0]}	48'd32985348833280	FTW1:
47:0	{reg151[15:0] ,reg16E[31:0]}	48'd65970697666560	FTW2:
47:0	{reg151[31:16],reg16F[31:0]}	48'd136339441844233	FTW3:
47:0	{reg156[15:0] ,reg152[31:0]}	48'd136339441844233	FTW4:
47:0	{reg156[31:16],reg153[31:0]}	48'd32985348833280	FTW5:
47:0	{reg157[15:0] ,reg154[31:0]}	48'd67114189759447	FTW6:
47:0	{reg157[31:16],reg155[31:0]}	48'd136339441844233	FTW7:

JESD204B APB 读写寄存器

表 12 JESD204B APB 寄存器地址映射

Begin Address	End Address	Range	module
0x00	0x7F	7bits	JESD204B MAC
0x80	0xFF	7bits	JESD204B PMA PHY

MAC Register

表 13 MAC Register

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x000	version_1	[7:0]	version_1		version number 1	0x20	R
0x001	version_2	[7:0]	version_2		version number 2	0x23	R
0x002	version_3	[7:0]	version_3		version number 3	0x05	R
0x003	version_4	[7:0]	version_4		version number 4	0x31	R
0x004	test	[7:0]	test_reg		reg for r/w test.	0x0	R/W
0x005	global_ctrl	[7]	PMA_pwrdn	0 1	204B IP power down control bit normal work power down	0x0	R/W
		[6:0]	Reserved		Reserved.	0x0	R
0x010	Sync mode	[7:3]	Reserved		Reserved.	0x0	R
		[2:1]	SYSREF± mode select	0 1 10	Disabled. Continuous. One-shot.	0x0	R/W
		[0]	Synchronization mode	1	Timestamp mode. The SYSREF signal does not reset internal clock dividers. In this mode, the JESD204B link and the signal monitor are not affected by the SYSREF signal. The SYSREF signal timestamps a sample as it passes through the ADC and is used as a control bit in the JESD204B output word.	0x0	R/W
0x011	sync error report	[7]	sync error cnt clear	0	1: clear error cnt	0x0	R/W
		[6:0]	sync error cnt	0	error cnt	0x0	R
0x012	User Pattern 1 LSB	[7:0]	User Pattern 1 [7:0]		User Test Pattern 1 least significant byte.	0x0	R/W
0x013	User Pattern 1 MSB	[7:0]	User Pattern 1 [15:8]		User Test Pattern 1 least significant byte.	0x0	R/W
0x014	User Pattern 2 LSB	[7:0]	User Pattern 2 [7:0]		User Test Pattern 2 least significant byte.	0x0	R/W
0x015	User Pattern 2 MSB	[7:0]	User Pattern 2 [15:8]		User Test Pattern 2 least significant byte.	0x0	R/W
0x016	User Pattern 3 LSB	[7:0]	User Pattern 3 [7:0]		User Test Pattern 3 least significant bits.	0x0	R/W
0x017	User Pattern 3 MSB	[7:0]	User Pattern 3 [15:8]		User Test Pattern 3 least significant bits.	0x0	R/W
0x018	User Pattern 4 LSB	[7:0]	User Pattern 4 [7:0]		User Test Pattern 4 least significant bits.	0x0	R/W
0x019	User Pattern 4 MSB	[7:0]	User Pattern 4 [15:8]		User Test Pattern 4 least significant bits.	0x0	R/W
0x01A	Output Mode Control	[7:6]	Reserved		Reserved.	0x0	R/W
		[5:4]	Converter control Bit 2 selection	0 1 10 11	Tie low (1'b0). control bit0 SYSREF Tie high(1'b1).	0x0	R/W
		[3:2]	Converter control Bit 1 selection	0 1 10 11	Tie low (1'b0). control bit0 SYSREF Tie high(1'b1).	0x0	R/W
		[1:0]	Converter control Bit 0 selection	0 1 10 11	Tie low (1'b0). control bit0 SYSREF Tie high(1'b1).	0x0	R/W

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x01B	PLL control	[7:4]	JESD204B lane rate control	0000 0001 0010 0011 0100 0101 0110	13.5~17G 8.5~13.5G 6.75~8.5G 4.25~6.75G 3.375~4.25G 2.125~3.375G 1.6875~2.125G	0x0	R/W
		[3:0]	ADC_num	0000 0001 0010	1 adc 2 adc 4 adc	0x0	R/W
0x01C	PLL status	[7]	clear_loss_lock	0 1	no action clear bit[1]	0x0	R/W
		[6:2]	Reserved	0	Reserved.	0x0	R
		[1]	PLL loss of lock	1	Loss of lock sticky bit. Indicate a loss of lock has occurred at some time. Cleared by setting bit[7].	0x0	R
		[0]	PLL lock status	0 1	Not locked. Locked.	0x0	R
0x01D	JESD204B Link status	[7:3]	Reserved		Reserved.	0x0	R
		[2]	sysref_sync_done		received sysref signal	0x0	R
		[1]	link_ready		pma fsm reset done	0x0	R
		[0]	tx_ready		clk_char&clk_samp reset done.	0x0	R
0x01E	pdiv/debug_ctrl	[5]	Reserved	0	Reserved.		
		[5]	Reserved	0	Reserved.		
		[4]	Reserved	0	Reserved.		
		[3:0]	debug_sel		debug pin select control	0x0	R/W
0x01F	DCM	[7]	Reserved	0	Reserved.		
		[6:0]	DCM	0000000 0000001 0000010 1111.1..1. 0.. 1111111	Decimation ratio = 1. Decimation ratio = 2. Decimation ratio = 3. D...e..c.imation ratio = 127. Decimation ratio = 128.		
0x020	JESD204B Link Control 1	[7]	Standby mode	0 1	Standby mode forces zeros for all converter samples. Standby mode forces code group synchronization (K28.5 characters).	0x0	R/W
		[6]	Tail bit(t) PN	0 1	Disable. Enable.	0x0	R/W
		[5]	Syncb_error_disable	0 1	Subclass 1 or Subclass 2 receiver devices shall indicate the detection of such an error by activating the SYNC~ signal for exactly 2 frame periods. Disable.	0x0	R/W
		[4]	Lane synchronization	0 1	Disable FACI uses /K28.7/. Enable FACI uses /K28.3/ and /K28.7/.	0x1	R/W
		[3:2]	ILAS sequence mode	00 01 11	Initial lane alignment sequence disabled (JESD204B Section 5.3.3.5). Initial lane alignment sequence enabled (JESD204B Section 5.3.3.5). Initial lane alignment sequence always on test mode. JESD204B data link layer test mode where repeated lane alignment sequence (as specified in JESD204B Section 5.3.3.8.2) sent on all lanes.	0x1	R/W
		[1]	FACI	0 1	Frame alignment character insertion enabled (JESD204B Section 5.3.3.4). Frame alignment character insertion disabled. For debug only (JESD204B Section 5.3.3.4).	0x0	R/W
		[0]	Link control	0 1	JESD204B serial transmit link enabled. Transmission of the /K28.5/ characters for code group synchronization is controlled by the SYNC~ signal. JESD204B serial transmit link powered down (held in reset and clock gated).	0x0	R/W

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x021	JESD204B Link Control 2	[7:6]	SYNCINB± pin control	0 10 11	Normal mode. Ignore SYNCINB± (force CGS). Ignore SYNCINB± (force ILAS/user data).	0x0	R/W
		[5]	SYNCINB± pin invert	0 1	SYNCINB± pin not inverted. SYNCINB± pin inverted.	0x0	R/W
		[4]	Long transport layer test	0 1	JESD204B test samples disabled. JESD204B test samples enabled; long transport layer test sample sequence (as specified in JESD204B Section 5.1.6.3) sent on all link lanes.	0x0	R/W
		[3]	Short transport layer test	0 1	JESD204B test samples disabled. JESD204B test samples enabled; long transport layer test sample sequence (as specified in JESD204B Section 5.1.6.2) sent on all link lanes.	0x0	R/W
		[2]	8-bit/10-bit bypass	0 1	8-bit/10-bit enabled. 8-bit/10-bit bypassed (most significant 2 bits are 0).	0x0	R/W
		[1]	8-bit/10-bit bit invert	0 1	Normal. Invert a, b, c, d, e, f, g, h, I, and j symbols.	0x0	R/W
		[0]	link standby	0 1	Normal mode Link standby mode, clock is on, but only transimit K28.5 code.	0x0	R/W
0x022	JESD204B Link Control 3	[7:6]	Checksum mode	0 1 10 11	Checksum is the sum of all 8-bit registers in the link configuration table. Checksum is the sum of all individual link configuration fields (LSB aligned). Checksum is disabled (set to zero). For test purposes only. Unused.	0x1	R/W
		[5:4]	Test injection point	0 1 10	N' sample input. 10-bit data at 8-bit/10-bit output (for PHY testing). 8-bit data at scrambler input.	0x0	R/W
		[3:0]	JESD204B test mode patterns	0 1 10 11 100 101 110 111 1000 1110 1111	Normal operation (test mode disabled). Alternating checkerboard. 1/0 word toggle. 31-bit pseudorandom number (PN) sequence: x31 + x28 + 1. 23-bit PN sequence: x23 + x18 + 1. 15-bit PN sequence: x15 + x14 + 1. 9-bit PN sequence: x9 + x5 + 1. 7-bit PN sequence: x7 + x6 + 1. Ramp output. Continuous/repeat user test. Single user test.	0x0	R/W

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x023	JESD204B Link Control 4	[7:4]	ILAS delay	0 1 10 11 100 101 110 111 1000 1001 1010 1011 1100 1101 1110 1111	Transmit ILAS on first LMFC after SYNCINB± deasserted. Transmit ILAS on second LMFC after SYNCINB± deasserted. Transmit ILAS on third LMFC after SYNCINB± deasserted. Transmit ILAS on fourth LMFC after SYNCINB± deasserted. Transmit ILAS on fifth LMFC after SYNCINB± deasserted. Transmit ILAS on sixth LMFC after SYNCINB± deasserted. Transmit ILAS on seventh LMFC after SYNCINB± deasserted. Transmit ILAS on eighth LMFC after SYNCINB± deasserted. Transmit ILAS on ninth LMFC after SYNCINB± deasserted. Transmit ILAS on tenth LMFC after SYNCINB± deasserted. Transmit ILAS on eleventh LMFC after SYNCINB± deasserted. Transmit ILAS on twelfth LMFC after SYNCINB± deasserted. Transmit ILAS on thirteenth LMFC after SYNCINB± deasserted. Transmit ILAS on fourteenth LMFC after SYNCINB± deasserted. Transmit ILAS on fifteenth LMFC after SYNCINB± deasserted. Transmit ILAS on sixteenth LMFC after SYNCINB± deasserted.	0x0	R/W
		[3]	Reserved		Reserved.	0x0	R
		[2:0]	Link layer test mode	0 1 10 11 100 101 110 111	Normal operation (link layer test mode disabled). Continuous sequence of /D21.5/ characters. Reserved. Reserved. Modified RPAT test sequence. JSPAT test sequence. JTSPAT test sequence. Reserved.	0x0	R/W
0x024	JESD204B LMFC offset	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	LMFC phase offset value		Local multiframeclock (LMFC) phase offset value (in frame clocks). Refer to the Deterministic Latency section.	0x0	R/W
0x025	JESD204B scrambling and number lanes (L) configuration	[7]	JESD204B scrambling (SCR)	0 1	JESD204B scrambler disabled (SCR = 0). JESD204B scrambler enabled (SCR = 1).	0x1	R/W
		[6:5]	Reserved		Reserved.	0x0	R
		[4:0]	JESD204B lanes (L)	0 1 11 111…1	One lane per link (L = 1). Two lanes per link (L = 2). Four lanes per link (L = 4). Eight lanes per Link (L = 16).	0xB	R/W
0x026	JESD204B link number of octets per frames (F)	[7:0]	JESD204B F configuration	0 1 10 11 101 111 1111	JESD204B number of octets per frame (F = JESD204B F configuration + 1) F = 1. F = 2. F = 3. F = 4. F = 6. F = 8. F = 16.	0x1	R/W
0x027	JESD204B link number of frames per multiframe (K)	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	JESD204B K configuration		JESD204B number of frames per multiframe (K = JESD204B K configuration + 1). Only values where F × K is divisible by 4 can be used.	0x1F	R/W

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x028	JESD204B link number of converters (M)	[7:0]	JESD204B M configuration	0 1 11 111	JESD204B number of converters per link/device (M = JESD204B M configuration). Link connected to one virtual converter (M = 1). Link connected to two virtual converters (M = 2). Link connected to four virtual converters (M = 4). Link connected to eight virtual converters (M = 8).	0x0	R/W
0x029	JESD204B number of control bits (CS) and ADC resolution (N)	[7:6]	Number of control bits (CS) per sample	0 1 10 11	No control bits (CS = 0). 1 control bit (CS = 1), Control Bit 2 only. 2 control bits (CS = 2), Control Bit 2 and Control Bit 1 only. 3 control bits (CS = 3), all control bits (Control Bit 2, Control Bit 1, and Control Bit 0).	0x0	R/W
		[5]	Reserved		Reserved.	0x0	R
		[4:0]	ADC converter resolution (N)	110 111 1000 1001 1010 1011 1100 1101 1110 1111	N = 7-bit resolution. N = 8-bit resolution. N = 9-bit resolution. N = 10-bit resolution. N = 11-bit resolution. N = 12-bit resolution. N = 13-bit resolution. N = 14-bit resolution. N = 15-bit resolution. N = 16-bit resolution.	0xB	R/W
0x02A	JESD204B SCV NP configuration	[7:5]	Subclass support	0 1	Subclass 0. Subclass 1.	0x0	R/W
		[4:0]	ADC number of bits per sample(N')	111 1011 1111	' = N 8. ' = N 12. ' = N 16.	0xB	R/W
0x02B	JESD204B JV S configuration	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Samples per converter frame cycle (S)		Samples per converter frame cycle (S = Register 0x0591, Bits[4:0] + 1).	0xF	R
0x02C	JESD204B HD CF configuration	[7]	HD value	0 1	High density format disabled. High density format enabled.	0x1	R
		[6:5]	Reserved		Reserved.	0x0	R
		[4:0]	Control words per frame clock cycle per link (CF)		Number of control words per frame clock cycle per link. (CF = 0)	0x0	R
0x02D	JESD204B DID configuration	[7:0]	JESD204B Tx DID value		JESD204B serial device identification (DID) number.	0x0	R/W
0x02E	JESD204B BID configuration	[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	JESD204B Tx BID value		JESD204B serial bank identification (BID) number (extension to DID).	0x0	R/W
0x030	JESD204B LID0 configuration	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Lane 0 LID value		JESD204B serial lane identification (LID) number for Lane 0.	0x0	R/W
0x031	JESD204B LID1 configuration	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Lane 1 LID value		JESD204B serial lane identification (LID) number for Lane 1.	0x1	R/W
0x032	JESD204B LID2 configuration	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Lane 2 LID value		JESD204B serial lane identification (LID) number for Lane 2.	0x2	R/W
0x033	JESD204B LID3 configuration	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Lane 3 LID value		JESD204B serial lane identification (LID) number for Lane 3.	0x3	R/W
0x034	JESD204B LID4 configuration	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Lane 4 LID value		JESD204B serial lane identification (LID) number for Lane 4.	0x4	R/W

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x035	JESD204B LID5 configuration	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Lane 5 LID value		JESD204B serial lane identification (LID) number for Lane 5.	0x5	R/W
0x036	JESD204B LID6 configuration	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Lane 6 LID value		JESD204B serial lane identification (LID) number for Lane 6.	0x6	R/W
0x037	JESD204B LID7 configuration	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Lane 7 LID value		JESD204B serial lane identification (LID) number for Lane 7.	0x7	R/W
0x038	JESD204B LID8 configuration	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Lane 8 LID value		JESD204B serial lane identification (LID) number for Lane 8.	0x8	R/W
0x039	JESD204B LID9 configuration	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Lane 9 LID value		JESD204B serial lane identification (LID) number for Lane 9.	0x9	R/W
0x03A	JESD204B LID10 configuration	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Lane 10 LID value		JESD204B serial lane identification (LID) number for Lane 10.	0xA	R/W
0x03B	JESD204B LID11 configuration	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Lane 11 LID value		JESD204B serial lane identification (LID) number for Lane 11.	0xB	R/W
0x03C	JESD204B LID12 configuration	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Lane 12 LID value		JESD204B serial lane identification (LID) number for Lane 12.	0xC	R/W
0x03D	JESD204B LID13 configuration	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Lane 13 LID value		JESD204B serial lane identification (LID) number for Lane 13.	0xD	R/W
0x03E	JESD204B LID14 configuration	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Lane 14 LID value		JESD204B serial lane identification (LID) number for Lane 14.	0xE	R/W
0x03F	JESD204B LID15 configuration	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Lane 15 LID value		JESD204B serial lane identification (LID) number for Lane 15.	0xF	R/W
0x040	JESD204B Lane Assign 1	[7:4]	SERDOUT1± lane assignment	0 1 10 11 100 101 x 1111	Physical Lane 1 assignment. Logical Lane 0. Logical Lane 1 (default). Logical Lane 2. Logical Lane 3. Logical Lane 4. Logical Lane 5. Logical Lane x. Logical Lane 15.	0x1	R/W
		[3:0]	SERDOUT0± lane assignment	0 1 10 11 100 101 x 1111	Physical Lane 0 assignment. Logical Lane 0 (default). Logical Lane 1. Logical Lane 2. Logical Lane 3. Logical Lane 4. Logical Lane 5. Logical Lane x. Logical Lane 15.	0x0	R/W
0x041	JESD204B Lane Assign 2	[7:4]	SERDOUT3± lane assignment	0 1 10 11 100 101 x 1111	Physical Lane 3 assignment. Logical Lane 0. Logical Lane 1. Logical Lane 2. Logical Lane 3 (default). Logical Lane 4. Logical Lane 5. Logical Lane x. Logical Lane 15.	0x3	R/W
		[3:0]	SERDOUT2± lane assignment	0 1 10 11 100 101 x 1111	Physical Lane 2 assignment. Logical Lane 0. Logical Lane 1 Logical Lane 2 (default). Logical Lane 3. Logical Lane 4. Logical Lane 5. Logical Lane x. Logical Lane 15.	0x2	R/W

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x042	JESD204B Lane Assign 3	[7:4]	SERDOUT5± lane assignment	0 1 10 11 100 101 x 1111	Physical Lane 5 assignment. Logical Lane 0. Logical Lane 1. Logical Lane 2. Logical Lane 3. Logical Lane 4. Logical Lane 5 (default). Logical Lane x. Logical Lane 15.	0x5	R/W
		[3:0]	SERDOUT4± lane assignment	0 1 10 11 100 101 x 1111	Physical Lane 4 assignment. Logical Lane 0. Logical Lane 1. Logical Lane 2. Logical Lane 3. Logical Lane 4 (default). Logical Lane 5. Logical Lane x. Logical Lane 15.	0x4	R/W
0x043	JESD204B Lane Assign 4	[7:4]	SERDOUT7± lane assignment	0 1 10 11 100 x 111 1111	Physical Lane 7 assignment. Logical Lane 0. Logical Lane 1. Logical Lane 2. Logical Lane 3. Logical Lane 4. Logical Lane x. Logical Lane 7 (default). Logical Lane 15.	0x7	R/W
		[3:0]	SERDOUT6± lane assignment	0 1 10 11 100 x 110 1111	Physical Lane 6 assignment. Logical Lane 0. Logical Lane 1. Logical Lane 2. Logical Lane 3. Logical Lane 4. Logical Lane x. Logical Lane 6 (default). Logical Lane 15.	0x6	R/W
0x044	JESD204B Lane Assign 5	[7:4]	SERDOUT9± lane assignment	0 1 10 11 100 x 1001 1111	Physical Lane 9 assignment. Logical Lane 0. Logical Lane 1. Logical Lane 2. Logical Lane 3. Logical Lane 4. Logical Lane x. Logical Lane 9 (default). Logical Lane 15.	0x9	R/W
		[3:0]	SERDOUT8± lane assignment	0 1 10 11 100 x 1000 1111	Physical Lane 8 assignment. Logical Lane 0. Logical Lane 1. Logical Lane 2. Logical Lane 3. Logical Lane 4. Logical Lane x. Logical Lane 8 (default). Logical Lane 15.	0x8	R/W
0x045	JESD204B Lane Assign 6	[7:4]	SERDOUT11± lane assignment	0 1 10 11 100 x 1011 1111	Physical Lane 11 assignment. Logical Lane 0. Logical Lane 1. Logical Lane 2. Logical Lane 3. Logical Lane 4. Logical Lane x. Logical Lane 11 (default). Logical Lane 15.	0xB	R/W
		[3:0]	SERDOUT10± lane assignment	0 1 10 11 100 x 1010 1111	Physical Lane 10 assignment. Logical Lane 0. Logical Lane 1. Logical Lane 2. Logical Lane 3. Logical Lane 4. Logical Lane x. Logical Lane 10 (default). Logical Lane 15.	0xA	R/W

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x046	JESD204B Lane Assign 7	[7:4]	SERDOUT13± lane assignment	0 1 10 11 100 x 1101 1111	Physical Lane 13 assignment. Logical Lane 0. Logical Lane 1. Logical Lane 2. Logical Lane 3. Logical Lane 4. Logical Lane x. Logical Lane 13 (default). Logical Lane 15.	0xD	R/W
		[3:0]	SERDOUT12± lane assignment	0 1 10 11 100 x 1100 1111	Physical Lane 12 assignment. Logical Lane 0. Logical Lane 1. Logical Lane 2. Logical Lane 3. Logical Lane 4. Logical Lane x. Logical Lane 12 (default). Logical Lane 15.	0xC	R/W
0x047	JESD204B Lane Assign 7	[7:4]	SERDOUT15± lane assignment	0 1 10 11 100 x 1110 1111	Physical Lane 15 assignment. Logical Lane 0. Logical Lane 1. Logical Lane 2. Logical Lane 3. Logical Lane 4. Logical Lane x. Logical Lane 14. Logical Lane 15 (default).	0xF	R/W
		[3:0]	SERDOUT14± lane assignment	0 1 10 11 100 x 1110 1111	Physical Lane 14 assignment. Logical Lane 0. Logical Lane 1. Logical Lane 2. Logical Lane 3. Logical Lane 4. Logical Lane x. Logical Lane 14 (default). Logical Lane 15.	0xE	R/W
0x048	SERDOUTx± data invert	[7]	Invert SERDOUT7± data	0 1	Invert SERDOUT7± data. Normal. Invert.	0x0	R/W
		[6]	Invert SERDOUT6± data	0 1	Invert SERDOUT6± data. Normal. Invert.	0x0	R/W
		[5]	Invert SERDOUT5± data	0 1	Invert SERDOUT5± data. Normal. Invert.	0x0	R/W
		[4]	Invert SERDOUT4± data	0 1	Invert SERDOUT4± data. Normal. Invert.	0x0	R/W
		[3]	Invert SERDOUT3± data	0 1	Invert SERDOUT3± data. Normal. Invert.	0x0	R/W
		[2]	Invert SERDOUT2± data	0 1	Invert SERDOUT2± data. Normal. Invert.	0x0	R/W
		[1]	Invert SERDOUT1± data	0 1	Invert SERDOUT1± data. Normal. Invert.	0x0	R/W
		[0]	Invert SERDOUT0± data	0 1	Invert SERDOUT0± data. Normal. Invert.	0x0	R/W

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x049	SERDOUTx± data invert	[7]	Invert SERDOUT15± data	0 1	Invert SERDOUT15± data. Normal. Invert.	0x0	R/W
		[6]	Invert SERDOUT14± data	0 1	Invert SERDOUT14± data. Normal. Invert.	0x0	R/W
		[5]	Invert SERDOUT13± data	0 1	Invert SERDOUT13± data. Normal. Invert.	0x0	R/W
		[4]	Invert SERDOUT12± data	0 1	Invert SERDOUT12± data. Normal. Invert.	0x0	R/W
		[3]	Invert SERDOUT11± data	0 1	Invert SERDOUT11± data. Normal. Invert.	0x0	R/W
		[2]	Invert SERDOUT10± data	0 1	Invert SERDOUT10± data. Normal. Invert.	0x0	R/W
		[1]	Invert SERDOUT9± data	0 1	Invert SERDOUT9± data. Normal. Invert.	0x0	R/W
		[0]	Invert SERDOUT8± data	0 1	Invert SERDOUT8± data. Normal. Invert.	0x0	R/W
0x050	JESD204B Checksum 0 configuration	[7:0]	lane0_chksum		Serial checksum value for Lane 0. Automatically calculated for each lane. Sum (all link configuration parameters for Lane 0) mod 256.		R
0x051	JESD204B Checksum 1 configuration	[7:0]	lane1_chksum		Serial checksum value for Lane 1. Automatically calculated for each lane. Sum (all link configuration parameters for Lane 1) mod 256.		R
0x052	JESD204B Checksum 2 configuration	[7:0]	lane2_chksum		Serial checksum value for Lane 2. Automatically calculated for each lane. Sum (all link configuration parameters for Lane 2) mod 256.		R
0x053	JESD204B Checksum 3 configuration	[7:0]	lane3_chksum		Serial checksum value for Lane 3. Automatically calculated for each lane. Sum (all link configuration parameters for Lane 3) mod 256.		R
0x054	JESD204B Checksum 4 configuration	[7:0]	lane4_chksum		Serial checksum value for Lane 4. Automatically calculated for each lane. Sum (all link configuration parameters for Lane 4) mod 256.		R
0x055	JESD204B Checksum 5 configuration	[7:0]	lane5_chksum		Serial checksum value for Lane 5. Automatically calculated for each lane. Sum (all link configuration parameters for Lane 5) mod 256.		R
0x056	JESD204B Checksum 6 configuration	[7:0]	lane6_chksum		Serial checksum value for Lane 6. Automatically calculated for each lane. Sum (all link configuration parameters for Lane 6) mod 256.		R
0x057	JESD204B Checksum 7 configuration	[7:0]	lane7_chksum		Serial checksum value for Lane 7. Automatically calculated for each lane. Sum (all link configuration parameters for Lane 7) mod 256.		R
0x058	JESD204B Checksum 8 configuration	[7:0]	lane8_chksum		Serial checksum value for Lane 8. Automatically calculated for each lane. Sum (all link configuration parameters for Lane 8) mod 256.		R
0x059	JESD204B Checksum 9 configuration	[7:0]	lane9_chksum		Serial checksum value for Lane 9. Automatically calculated for each lane. Sum (all link configuration parameters for Lane 9) mod 256.		R
0x05A	JESD204B Checksum 10 configuration	[7:0]	lane10_chksum		Serial checksum value for Lane 10. Automatically calculated for each lane. Sum (all link configuration parameters for Lane 10) mod 256.		R
0x05B	JESD204B Checksum 11 configuration	[7:0]	lane11_chksum		Serial checksum value for Lane 11. Automatically calculated for each lane. Sum (all link configuration parameters for Lane 11) mod 256.		R
0x05C	JESD204B Checksum 12 configuration	[7:0]	lane12_chksum		Serial checksum value for Lane 12. Automatically calculated for each lane. Sum (all link configuration parameters for Lane 12) mod 256.		R

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x05D	JESD204B Checksum 13 configuration	[7:0]	lane13_chksum		Serial checksum value for Lane 13. Automatically calculated for each lane. Sum (all link configuration parameters for Lane 13) mod 256.		R
0x05E	JESD204B Checksum 14 configuration	[7:0]	lane14_chksum		Serial checksum value for Lane 14. Automatically calculated for each lane. Sum (all link configuration parameters for Lane 14) mod 256.		R
0x05F	JESD204B Checksum 15 configuration	[7:0]	lane15_chksum		Serial checksum value for Lane 15. Automatically calculated for each lane. Sum (all link configuration parameters for Lane 15) mod 256.		R
0x60	PMA fifo wr enable	[7:0]	dbg_fifo_wr[7:0]		fifo wr enable for lane 0~7		R
0x61	PMA fifo wr enable	[7:0]	dbg_fifo_wr[15:8]		fifo wr enable for lane 8~15		R
0x62	PMA fifo rd enable	[7:0]	dbg_fifo_rd[7:0]		fifo rd enable for lane 0~7		R
0x63	PMA fifo rd enable	[7:0]	dbg_fifo_rd[15:8]		fifo rd enable for lane 8~15		R
0x64	PMA fifo empty	[7:0]	dbg_fifo_empty[7:0]		fifo empty for lane 0~7		R
0x65	PMA fifo empty	[7:0]	dbg_fifo_empty[15:8]		fifo empty for lane 8~15		R
0x66	PMA fifo full	[7:0]	dbg_fifo_full[7:0]		fifo full for lane 0~7		R
0x67	PMA fifo full	[7:0]	dbg_fifo_full[15:8]		fifo full for lane 8~15		R
0x68	PMA ready	[7:0]	dbg_pma_ready[7:0]		pma ready for lane 0~7		R
0x69	PMA ready	[7:0]	dbg_pma_ready[15:8]		pm ready for lane 8~15		R
0x6A	PMA fifo rd start	[7:0]	dbg_rd_start[7:0]		fifo rd start for lane 0~7		R
0x6B	PMA fifo rd start	[7:0]	dbg_rd_start[15:8]		fifo rd start for lane 8~15		R
0x6C	PMA fifo wr start	[7:6]	Reserved		Reserved.		R
		[0]	dbg_wr_start		fifo write start for all lanes		R

PMA PHY Register

表 14 PMA PHY Register

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x00	pll_cfg0	[7:0]	JESD204B pll cfg0			8'b0111,0101	R/W
		[7:5]	pll_cp_itrim	011	cp current trimming bits 3'b000: 50u 3'b001:100u 3'b010:150u 3'b011:200u default 3'b100:250u 3'b101:300u 3'b110:350u 3'b111:400u		R/W
		[4:3]	pll_cp_rsv	10	cp reset voltage trimming bits 2'b00: (1-12.5%)*vrst voltage 2'b01: (1-6.25%)*vrst voltage 2'b10: vrstvoltage default 2'b11: (1+6.25%)*vrst voltage		R/W
		[2:1]	pll_cp_ls	10	cp level shift voltage trimming bits 2'b00: (1+12.5%)*vls voltage 2'b01: vls voltage 2'b10: vls voltage 2'b11: (1+12.5%)*vls voltage		R/W
		[0]	pll_lock_en	1	pll lock detect enable 1'b0: disable 1'b1: enable		R/W
0x01	pll_cfg1	[7:0]	JESD204B pll cfg1			8'b1010,1010	R/W
		[7:5]	pll_lpf_rtrim	101	lpf resistor trimming bits 3'b000: 10k 3'b001: 9k 3'b010: 8k 3'b011: 7k 3'b100: 6k 3'b101: 5k default 3'b110: 4k 3'b111: 3k		R/W
		[4:3]	pll_div2_itrim	01	high speed div2 current trimming bits 2'b00: 1.6mA 2'b01: 2mA 2'b10: 2.4mA 2'b11: 2.8mA		R/W
		[2:1]	pll_div2_buf	01	high speed div2buf current trimming bits 2'b00: 2mA 2'b01: 3mA 2'b10: 3mA 2'b11: 4mA		R/W
		[0]	RSV	0	Reserved		R/W
0x02	pll_cfg2	[7:0]	JESD204B pll cfg2			8'b0100,0010	R/W
		[7]	pll_vco_rtrim_mannul	0	pll vco rtrim mannul trimming bit 1'b0: auto mode 1'b1: mannul mode		
		[6:2]	pll_vco_rtrim_reg	10000	pll vco rtrim code in mannul mode		
		[1:0]	pll_fbdiv<1:0>	10	pll feedback divider ratio trimming bits 2'b00: /16 2'b01: /32 2'b10: /20 default 2'b11: /40		

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x03	pll_cfg3	[7:0]	JESD204B pll cfg3			8'b0001,0100	R/W
		[7]	pll_tsten	0	pll test enable 1'b0: disable 1'b1: enable		
		[6:5]	pll_atest_sel	00	pll analog voltage select 2'b00: no select 2'b01: select ldo voltage output 2'b10: select vcntl voltage output		
		[4:3]	pll_lock_factor	10	pll lock detect frequency compare mask select 2'b00:16'b1111 1111 1111 1000 2'b01:16'b1111 1111 1111 0000 2'b10:16'b1111 1111 1110 0000 default 2'b11:16'b1111 1111 1100 0000		
		[2:1]	pll_lock_coarse	10	pll lock detect frequency compare counter select 2'b00:16'd65535 2'b01:16'd4095 2'b10:16'd1023 default 2'b11:16'd255		
		[0]	RSV	0	Reserved		
0x04	pll_cfg4	[7:0]	JESD204B pll cfg4			8'b0100,0001	R/W
		[7]	pll_vco_crs_ovrden	0	vco code overwrite enable 1'0：disable 1'b1: enable		
		[6:1]	pll_vco_code	100000	vco overwrite code, mannul mode		
		[0]	pll_vco_ofst_en	1	ignore vco code offset enable 1'b0: disable, vco code with offset 1'b1: enable, ignore offset		
0x05	pll_cfg5	[7:0]	JESD204B pll cfg5			8'0001,1001	R/W
		[7]	pll_vco_band_sel	0	vco high band and low band select in mannul mode 1'b0：select high band 1'b1: select low band		
		[6:5]	pll_vco_accuracy	00	vco calibration perilod select 2b'00: 4095 default 2b'01: 1023 2b'10: 16383 2b'11: 65535		
		[4]	pll_vco_band_sel_auto	1	auto select vco high band and low band 1'b0：mannul mode 1'b1: auto mode		
		[3:2]	pll_vco_offset	10	offset of the vco coarse tuning code setting 2b'00: -1 2b'01: -2 2b'10: +1 2b'11: +2		
		[1:0]	pll_lock_latency_sel	01	waiting time trimming when pll in the closed loop pll 2b'00: 65535 2b'01: 16383 default 2b'10: 4095 2b'11: 1023		

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x06	rcal_cfg0	[7:0]	JESD204B rcalcfg0			8'b0101,0110	R/W
		[7:6]	ircal50u_cal_ctl	01	current trimming for the resistor calibration block 2'b00:1mA*98% 2'b01:1mA 2'b10:1mA*1.02% 2'b11:1mA*1.04%		
		[5:4]	ircal50u_pll_ctl	01	pll calibration current trimming bits for 50u 2'b00:45u 2'b01:50u 2'b10:55u 2'b11:60u		
		[3:2]	ircal50u_tx_ctl	01	tx calibration current trimming bits for 50u 2'b00:45u 2'b01:50u 2'b10:55u 2'b11:60u		
		[1]	rcalenb_manual	1	resistor calibration mode 1'b0: manual mode 1'b1:auto mode		
		[0]	iref_testen	0	test enable for accurate 50u current for adc core 1'b0: disable 1'b1: enable		
0x07	rcal_cfg1	[7:0]	JESD204B rcal cfg1			8'b0000,0000	R/W
		[7:5]	txcal_offset	000	tx calibration code offset 3'b000: rcal _tx[4:0]= rcal[4:0] 3'b001: rcal _tx[4:0]= rcal[4:0]+1 3'b010: rcal _tx[4:0]= rcal[4:0]+2 3'b011: rcal _tx[4:0]= rcal[4:0]+3 3'b100: rcal _tx[4:0]= rcal[4:0] 3'b101: rcal _tx[4:0]= rcal[4:0]-1 3'b110: rcal _tx[4:0]= rcal[4:0]-2 3'b111: rcal _tx[4:0]= rcal[4:0]-3		
		[4:2]	pllcal_offset	000	pll calibration code offset 3'b000: rcal _pll[4:0]= rcal[4:0] 3'b001: rcal _pll[4:0]= rcal[4:0]+1 3'b010: rcal _pll[4:0]= rcal[4:0]+2 3'b011: rcal _pll[4:0]= rcal[4:0]+3 3'b100: rcal _pll[4:0]= rcal[4:0] 3'b101: rcal _pll[4:0]= rcal[4:0]-1 3'b110: rcal _pll[4:0]= rcal[4:0]-2 3'b111: rcal _pll[4:0]= rcal[4:0]-3		
		[1:0]	RSV	00	Reserved		
0x08	tx_cfg0	[7:0]	JESD204B tx cfg0			8'b1110,0000	R/W
		[7:6]	tx_wide_mode, tx_divbyfive	11	tx data width select 2'b00: 16 bits 2'b01: 20 bits 2'b10: 32 bits 2'b11: 40 bits		
		[5:3]	tx_drvbiastrim	100	driver bias current trimming 3'b000: -40uA 3'b001: -30uA 3'b010: -20uA 3'b011: -10uA 3'b100: +0uA 3'b101: +10uA 3'b110: +20uA 3'b111: +30uA		
		[2:0]	tx_emppre	000	tx pre-cursor setting		
0x09	tx_cfg1	[7:0]	JESD204B tx cfg1			8'b1000,0000	R/W
		[7:3]	tx_termprog	10000	tx code manual		
		[2]	tx_dcc_enb	0	tx duty cycle calibration enable, active low 1'b0: enable 1'b1: disable		
		[1]	tx_termcodesel	0	tx code mode select 1'b0: auto mode 1'b1: manual mode		
		[0]	tx_termtest	0	tx term test		

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0A	tx_cfg2	[7:0]	JESD204B tx cfg2			8'b0000,0000	R/W
		[7]	tx_tstdiven	0	tx low speed data test enable 1'b0: disable 1'b1: enable		
		[6:3]	tx_amonsel	0000	tx analog test voltage select, detail see TestMux		
		[2]	tx_pdivsel<2>	0	tx post divider by 16 when it is enabled		
		[1]	tx_prbs_en	0	tx prbs enable 1'b0:disable 1'b1: enable		
		[0]	tx_prbs_mode	0	tx prbs mode select 1'b0: 0101 pattern 1'b1: prbs7 pattern		
0x0B	com_cfg0	[7:0]	JESD204B com cfg0			8'b0000,0000	R/W
		[7]	RSV	0	Reserved		
		[6]	com_dig_tst_sel	0	digital signal select 1'b0: select refclk for com_tstclk<0> /select fbclk for com_tstclk<1> 1'b1: select tielow for com_tstclk<0> /select cfgclk for com_tstclk<1>		
		[5:0]	com_ana_tst_sel	000000	analog signal select detail see TestMux		
0x0C	bg_cfg0	[7:0]	JESD204B bg cfg0			8'b0101,0101	R/W
		[7:6]	ir50u_pll_ctrl	01	vbg/r current of pll trimming bits for 50u 2'b00:45u 2'b01:50u 2'b10:55u 2'b11:60u		
		[5:4]	ir50u_buff_ctrl	01	vbg/r current of buffer trimming bits for 50u 2'b00:45u 2'b01:50u 2'b10:55u 2'b11:60u		
		[3:2]	ir50u_rcal_ctrl	01	vbg/r current of rcal trimming bits for 50u 2'b00:45u 2'b01:50u 2'b10:55u 2'b11:60u		
		[1:0]	ir50u_spare_ctrl	01	vbg/r current of spare trimming bits for 50u 2'b00:45u 2'b01:50u 2'b10:55u 2'b11:60u		
0x0D	bg_cfg1	[7:0]	JESD204B bg cfg1			8'b0110,0000	R/W
		[7:6]	bg_trimcom	01	vbg voltage trimming bits 2'b00:1.193v 2'b01:1.216v 2'b10:1.24v 2'b11:1.264v		
		[5:3]	bg_trimvco	100	vco voltage trimming bits 3'b000:1.119v 3'b001:1.144v 3'b010:1.168v 3'b011:1.193v 3'b100:1.216v 3'b101:1.24v 3'b110:1.264v 3'b111:1.288v		
		[2]	bg_safemode	0	bg safe mode enable 1'b0: normal mode 1'b1: safe mode		
		[1]	bg_testen	0	bg test enable 1'b0: disable 1'b1: enable		
		[0]	RSV	0	Reserved		

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0E	pma_top_ cfg0	[7:0]	JESD204B pma top cfg0			8'b1000,0000	R/W
		[7:6]	pma_top_buf_itrim	10	clock buffer trimming bits 2'b00: 2mA 2'b01: 3mA 2'b10: 3mA 2'b11: 4mA		
		[5]	RSV	0	Reserved		
		[4:0]	pma_top_clktst_sel	00000	pma top test signal select detail see TestMux		
0x0F	pma_top_ cfg1	[7:0]	JESD204B pma top cfg1			8'b0000,0001	R/W
		[7]	bg_pwrdn	0	bg power down enable 1'b0: normal work 1'b1: power down	.	
		[6]	pll_pwrdn	0	pll power down enable 1'b0: normal work 1'b1: power down		
		[5:4]	RSV	000000	Reserved		
		[3]	pllck_dccfix	0	pllck duty cycle calibration fixed function 1'b0: normal work 1'b1: dcc output fixed to an equal level		
		[2]	pllck_dccenb	0	pllck duty cycle calibration enable, active low 1'b0: normal work 1'b1: disable pllck dcc funciton		
		[1:0]	pllck_dcctrim	01	dcc current trimming bits 2'b00: 0.6mA 2'b01: 0.9mA 2'b10: 1.2mA 2'b11: 1.5mA		
0x10	adc_clk_s time	[7:0]	JESD204B adc clk wait time			8'b1000,0000	R/W
		[7:3]	cfg_clk_wait_time	10000	PMA reset sequence adc_clk stable time control bits: cycle = 2^adc_clk_stime 5'b00000: 1 cycles of Cfg_Clk; 5'b00001: 2^1 cycles of Cfg_Clk; 5'b00010: 2^2 cycles of Cfg_Clk; … .; 5'b10000: 2^16 cycles of Cfg_Clk; default … .; 5'b11111: 2^31 cycles of Cfg_Clk;		
		[2:0]	RSV	000	Reserved		
0x11	fsm_reset _seq	[7:0]	JESD204B fsm reset			8'b0000,0000	R/W
		[7]	top_seq_bypass	0	top sequence bypass 1'b0: normal work 1'b1: bypass		
		[6]	lnk_rdy	0	link_ready 1'b0: not ready 1'b1: link ready		
		[5]	rcal_enb	0	rcal enable,active low 1'b0: enable 1'b1: disable		
		[4]	pll_rstb	0	pll reset,active low 1'b0: reset 1'b1: normal work		
		[3]	tx_rstb	0	tx reset,active low 1'b0: reset 1'b1: normal work		
		[2]	rstb_d	0	mac reset,active low 1'b0: reset 1'b1: normal work		
		[1:0]	RSV	00	Reserved		

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x12	divider_cfg	[7:0]	JESD204B divider cfg in mannual			8'b0000,0000	R/W
		[7:6]	pll_mdiv	00	mdivider select config in mannual 2'b00: /1 2'b01: /2 2'b10: /4 2'b11: /8		
		[5:4]	tx_pdiv	00	pdivide select config in mannual 2'b00: /1 2'b01: /2 2'b10: /4 2'b11: /8		
		[3]	div_sel	0	1'b0: pll_mdiv/tx_pdiv use fsm value 1'b1: pll_mdiv/tx_pdivuse reg 0x12 bits [7:4].		
		[2]	adcdiv1	0	predivider in adc. 0: div 2 1: div 3		
		[1:0]	adcdiv0	00	predivider in adc. 00: div 1 01: div 2 10: div 4 11: div 8		
0x13	time_1us_set	[7:0]	time count for 1us			8'b1000,1010	R/W
		[7:0]	time_1us	1000,1010	timer count for 1.25us at 110MHz		
0x14	tx_pwr_cfg0	[7:0]	tx power down config			8'b0000,0000	R/W
		[7:0]	tx_pwrdn	0000,0000	tx power down 1'b0: normal work 1'b1: power down b..i.t<7>: control lane7 bit<0>: control lane0		
0x15	tx_pwr_cfg1	[7:0]	tx power down config			8'b0000,0000	R/W
		[7:0]	tx_pwrdn	0000,0000	tx power down 1'b0: normal work 1'b1: power down b..i.t<7>: control lane15 bit<0>: control lane8		
0x16	pll_status	[7:0]	pll status			8'b0000,0000	R
		[7]	RSV	0	Reserved		
		[6]	pll_afc_fine_en		pll fine tuning mode indicator 1'b0: coarse tuning process 1'b1: fine tuning process		
		[5:0]	pll_vco_ctrim		vco band code		
0x17	rcal_code	[7:0]	rcal code			8'b0000,0000	R
		[7:5]	RSV	00	Reserved		
		[4:0]	rcal_code		resistor calibration code		
0x20	tx_drvamp_cfg0	[7:0]	tx drvamp cfg0			8'b0100,0100	R/W
		[7]	RSV	0	Reserved		
		[6:4]	tx_drvamp_lane1	100	tx driver output amplitude control bits for lane1 3'b000 = 326 mV p-p, 3'b001 = 405 mV p-p, 3'b010 = 483 mV p-p, 3'b011 = 560 mV p-p, 3'b100 = 634 mV p-p, default 3'b101 = 704 mV p-p, 3'b110 = 768 mV p-p, 3'b111 reserved		
		[3]	RSV	0	Reserved		
		[2:0]	tx_drvamp_lane0	100	tx driver output amplitude control bits for lane0 3'b000 = 326 mV p-p, 3'b001 = 405 mV p-p, 3'b010 = 483 mV p-p, 3'b011 = 560 mV p-p, 3'b100 = 634 mV p-p, default 3'b101 = 704 mV p-p, 3'b110 = 768 mV p-p, 3'b111 reserved		

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x21	tx_drvamp_cfg1	[7:0]	tx drvamp cfg1			8'b0100,0100	R/W
		[7]	RSV	0	Reserved		
		[6:4]	tx_drvamp_lane3	100	tx driver output amplitude control bits for lane1 3'b000 = 326 mV p-p, 3'b001 = 405 mV p-p, 3'b010 = 483 mV p-p, 3'b011 = 560 mV p-p, 3'b100 = 634 mV p-p, default 3'b101 = 704 mV p-p, 3'b110 = 768 mV p-p, 3'b111 reserved		
		[3]	RSV	0	Reserved		
		[2:0]	tx_drvamp_lane2	100	tx driver output amplitude control bits for lane0 3'b000 = 326 mV p-p, 3'b001 = 405 mV p-p, 3'b010 = 483 mV p-p, 3'b011 = 560 mV p-p, 3'b100 = 634 mV p-p, default 3'b101 = 704 mV p-p, 3'b110 = 768 mV p-p, 3'b111 reserved		
0x22	tx_drvamp_cfg2	[7:0]	tx drvamp cfg2			8'b0100,0100	R/W
		[7]	RSV	0	Reserved		
		[6:4]	tx_drvamp_lane5	100	tx driver output amplitude control bits for lane1 3'b000 = 326 mV p-p, 3'b001 = 405 mV p-p, 3'b010 = 483 mV p-p, 3'b011 = 560 mV p-p, 3'b100 = 634 mV p-p, default 3'b101 = 704 mV p-p, 3'b110 = 768 mV p-p, 3'b111 reserved		
		[3]	RSV	0	Reserved		
		[2:0]	tx_drvamp_lane4	100	tx driver output amplitude control bits for lane0 3'b000 = 326 mV p-p, 3'b001 = 405 mV p-p, 3'b010 = 483 mV p-p, 3'b011 = 560 mV p-p, 3'b100 = 634 mV p-p, default 3'b101 = 704 mV p-p, 3'b110 = 768 mV p-p, 3'b111 reserved		
0x23	tx_drvamp_cfg3	[7:0]	tx drvamp cfg3			8'b0100,0100	R/W
		[7]	RSV	0	Reserved		
		[6:4]	tx_drvamp_lane7	100	tx driver output amplitude control bits for lane1 3'b000 = 326 mV p-p, 3'b001 = 405 mV p-p, 3'b010 = 483 mV p-p, 3'b011 = 560 mV p-p, 3'b100 = 634 mV p-p, default 3'b101 = 704 mV p-p, 3'b110 = 768 mV p-p, 3'b111 reserved		
		[3]	RSV	0	Reserved		
		[2:0]	tx_drvamp_lane6	100	tx driver output amplitude control bits for lane0 3'b000 = 326 mV p-p, 3'b001 = 405 mV p-p, 3'b010 = 483 mV p-p, 3'b011 = 560 mV p-p, 3'b100 = 634 mV p-p, default 3'b101 = 704 mV p-p, 3'b110 = 768 mV p-p, 3'b111 reserved		

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x24	tx_drvamp_cfg4	[7:0]	tx drvamp cfg4			8'b0100,0100	R/W
		[7]	RSV	0	Reserved		
		[6:4]	tx_drvamp_lane9	100	tx driver output amplitude control bits for lane1 3'b000 = 326 mV p-p, 3'b001 = 405 mV p-p, 3'b010 = 483 mV p-p, 3'b011 = 560 mV p-p, 3'b100 = 634 mV p-p, default 3'b101 = 704 mV p-p, 3'b110 = 768 mV p-p, 3'b111 reserved		
		[3]	RSV	0	Reserved		
		[2:0]	tx_drvamp_lane8	100	tx driver output amplitude control bits for lane0 3'b000 = 326 mV p-p, 3'b001 = 405 mV p-p, 3'b010 = 483 mV p-p, 3'b011 = 560 mV p-p, 3'b100 = 634 mV p-p, default 3'b101 = 704 mV p-p, 3'b110 = 768 mV p-p, 3'b111 reserved		
0x25	tx_drvamp_cfg5	[7:0]	tx drvamp cfg5			8'b0100,0100	R/W
		[7]	RSV	0	Reserved		
		[6:4]	tx_drvamp_lane11	100	tx driver output amplitude control bits for lane1 3'b000 = 326 mV p-p, 3'b001 = 405 mV p-p, 3'b010 = 483 mV p-p, 3'b011 = 560 mV p-p, 3'b100 = 634 mV p-p, default 3'b101 = 704 mV p-p, 3'b110 = 768 mV p-p, 3'b111 reserved		
		[3]	RSV	0	Reserved		
		[2:0]	tx_drvamp_lane10	100	tx driver output amplitude control bits for lane0 3'b000 = 326 mV p-p, 3'b001 = 405 mV p-p, 3'b010 = 483 mV p-p, 3'b011 = 560 mV p-p, 3'b100 = 634 mV p-p, default 3'b101 = 704 mV p-p, 3'b110 = 768 mV p-p, 3'b111 reserved		
0x26	tx_drvamp_cfg6	[7:0]	tx drvamp cfg6			8'b0100,0100	R/W
		[7]	RSV	0	Reserved		
		[6:4]	tx_drvamp_lane13	100	tx driver output amplitude control bits for lane1 3'b000 = 326 mV p-p, 3'b001 = 405 mV p-p, 3'b010 = 483 mV p-p, 3'b011 = 560 mV p-p, 3'b100 = 634 mV p-p, default 3'b101 = 704 mV p-p, 3'b110 = 768 mV p-p, 3'b111 reserved		
		[3]	RSV	0	Reserved		
		[2:0]	tx_drvamp_lane12	100	tx driver output amplitude control bits for lane0 3'b000 = 326 mV p-p, 3'b001 = 405 mV p-p, 3'b010 = 483 mV p-p, 3'b011 = 560 mV p-p, 3'b100 = 634 mV p-p, default 3'b101 = 704 mV p-p, 3'b110 = 768 mV p-p, 3'b111 reserved		

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x27	tx_drvamp_cfg7	[7:0]	tx drvamp cfg7			8'b0100,0100	R/W
		[7]	RSV	0	Reserved		
		[6:4]	tx_drvamp_lane15	100	tx driver output amplitude control bits for lane1 3'b000 = 326 mV p-p, 3'b001 = 405 mV p-p, 3'b010 = 483 mV p-p, 3'b011 = 560 mV p-p, 3'b100 = 634 mV p-p, default 3'b101 = 704 mV p-p, 3'b110 = 768 mV p-p, 3'b111 reserved		
		[3]	RSV	0	Reserved		
		[2:0]	tx_drvamp_lane14	100	tx driver output amplitude control bits for lane0 3'b000 = 326 mV p-p, 3'b001 = 405 mV p-p, 3'b010 = 483 mV p-p, 3'b011 = 560 mV p-p, 3'b100 = 634 mV p-p, default 3'b101 = 704 mV p-p, 3'b110 = 768 mV p-p, 3'b111 reserved		
0x28	tx_post_tap_cfg0	[7:0]	tx post tap cfg0			8'b0000,0000	R/W
		[7]	RSV	0	Reserved		
		[6:4]	tx_post_tap_lane1	000	tx post tap level control for lane1 3'b000 = 0 dB 3'b001 = 1.1dB, 3'b010 = 2.4dB, 3'b011 = 3.9dB, 3'b100 = 5.8dB, 3'b101 = 8.2dB, 3'b110 = 11.5dB, 3'b111 reserved		
		[3]	RSV	0	Reserved		
		[2:0]	tx_post_tap_lane0	000	tx post tap level control for lane0 3'b000 = 0 dB 3'b001 = 1.1dB, 3'b010 = 2.4dB, 3'b011 = 3.9dB, 3'b100 = 5.8dB, 3'b101 = 8.2dB, 3'b110 = 11.5dB, 3'b111 reserved		
0x29	tx_post_tap_cfg1	[7:0]	tx post tap cfg1			8'b0000,0000	R/W
		[7]	RSV	0	Reserved		
		[6:4]	tx_post_tap_lane3	000	tx post tap level control for lane1 3'b000 = 0 dB 3'b001 = 1.1dB, 3'b010 = 2.4dB, 3'b011 = 3.9dB, 3'b100 = 5.8dB, 3'b101 = 8.2dB, 3'b110 = 11.5dB, 3'b111 reserved		
		[3]	RSV	0	Reserved		
		[2:0]	tx_post_tap_lane2	000	tx post tap level control for lane0 3'b000 = 0 dB 3'b001 = 1.1dB, 3'b010 = 2.4dB, 3'b011 = 3.9dB, 3'b100 = 5.8dB, 3'b101 = 8.2dB, 3'b110 = 11.5dB, 3'b111 reserved		

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x2A	tx_post_tap_cfg2	[7:0]	tx post tap cfg2			8'b0000,0000	R/W
		[7]	RSV	0	Reserved		
		[6:4]	tx_post_tap_lane5	000	tx post tap level control for lane1 3'b000 = 0 dB 3'b001 = 1.1dB, 3'b010 = 2.4dB, 3'b011 = 3.9dB, 3'b100 = 5.8dB, 3'b101 = 8.2dB, 3'b110 = 11.5dB, 3'b111 reserved		
		[3]	RSV	0	Reserved		
		[2:0]	tx_post_tap_lane4	000	tx post tap level control for lane0 3'b000 = 0 dB 3'b001 = 1.1dB, 3'b010 = 2.4dB, 3'b011 = 3.9dB, 3'b100 = 5.8dB, 3'b101 = 8.2dB, 3'b110 = 11.5dB, 3'b111 reserved		
0x2B	tx_post_tap_cfg3	[7:0]	tx post tap cfg3			8'b0000,0000	R/W
		[7]	RSV	0	Reserved		
		[6:4]	tx_post_tap_lane7	000	tx post tap level control for lane1 3'b000 = 0 dB 3'b001 = 1.1dB, 3'b010 = 2.4dB, 3'b011 = 3.9dB, 3'b100 = 5.8dB, 3'b101 = 8.2dB, 3'b110 = 11.5dB, 3'b111 reserved		
		[3]	RSV	0	Reserved		
		[2:0]	tx_post_tap_lane6	000	tx post tap level control for lane0 3'b000 = 0 dB 3'b001 = 1.1dB, 3'b010 = 2.4dB, 3'b011 = 3.9dB, 3'b100 = 5.8dB, 3'b101 = 8.2dB, 3'b110 = 11.5dB, 3'b111 reserved		
0x2C	tx_post_tap_cfg4	[7:0]	tx post tap cfg4			8'b0000,0000	R/W
		[7]	RSV	0	Reserved		
		[6:4]	tx_post_tap_lane9	000	tx post tap level control for lane1 3'b000 = 0 dB 3'b001 = 1.1dB, 3'b010 = 2.4dB, 3'b011 = 3.9dB, 3'b100 = 5.8dB, 3'b101 = 8.2dB, 3'b110 = 11.5dB, 3'b111 reserved		
		[3]	RSV	0	Reserved		
		[2:0]	tx_post_tap_lane8	000	tx post tap level control for lane0 3'b000 = 0 dB 3'b001 = 1.1dB, 3'b010 = 2.4dB, 3'b011 = 3.9dB, 3'b100 = 5.8dB, 3'b101 = 8.2dB, 3'b110 = 11.5dB, 3'b111 reserved		

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x2D	tx_post_tap_cfg5	[7:0]	tx post tap cfg5			8'b0000,0000	R/W
		[7]	RSV	0	Reserved		
		[6:4]	tx_post_tap_lane11	000	tx post tap level control for lane1 3'b000 = 0 dB 3'b001 = 1.1dB, 3'b010 = 2.4dB, 3'b011 = 3.9dB, 3'b100 = 5.8dB, 3'b101 = 8.2dB, 3'b110 = 11.5dB, 3'b111 reserved		
		[3]	RSV	0	Reserved		
		[2:0]	tx_post_tap_lane10	000	tx post tap level control for lane0 3'b000 = 0 dB 3'b001 = 1.1dB, 3'b010 = 2.4dB, 3'b011 = 3.9dB, 3'b100 = 5.8dB, 3'b101 = 8.2dB, 3'b110 = 11.5dB, 3'b111 reserved		
0x2E	tx_post_tap_cfg6	[7:0]	tx post tap cfg6			8'b0000,0000	R/W
		[7]	RSV	0	Reserved		
		[6:4]	tx_post_tap_lane13	000	tx post tap level control for lane1 3'b000 = 0 dB 3'b001 = 1.1dB, 3'b010 = 2.4dB, 3'b011 = 3.9dB, 3'b100 = 5.8dB, 3'b101 = 8.2dB, 3'b110 = 11.5dB, 3'b111 reserved		
		[3]	RSV	0	Reserved		
		[2:0]	tx_post_tap_lane12	000	tx post tap level control for lane0 3'b000 = 0 dB 3'b001 = 1.1dB, 3'b010 = 2.4dB, 3'b011 = 3.9dB, 3'b100 = 5.8dB, 3'b101 = 8.2dB, 3'b110 = 11.5dB, 3'b111 reserved		
0x2F	tx_post_tap_cfg7	[7:0]	tx post tap cfg7			8'b0000,0000	R/W
		[7]	RSV	0	Reserved		
		[6:4]	tx_post_tap_lane15	000	tx post tap level control for lane1 3'b000 = 0 dB 3'b001 = 1.1dB, 3'b010 = 2.4dB, 3'b011 = 3.9dB, 3'b100 = 5.8dB, 3'b101 = 8.2dB, 3'b110 = 11.5dB, 3'b111 reserved		
		[3]	RSV	0	Reserved		
		[2:0]	tx_post_tap_lane14	000	tx post tap level control for lane0 3'b000 = 0 dB 3'b001 = 1.1dB, 3'b010 = 2.4dB, 3'b011 = 3.9dB, 3'b100 = 5.8dB, 3'b101 = 8.2dB, 3'b110 = 11.5dB, 3'b111 reserved		

9. 封装尺寸（Package Outline）

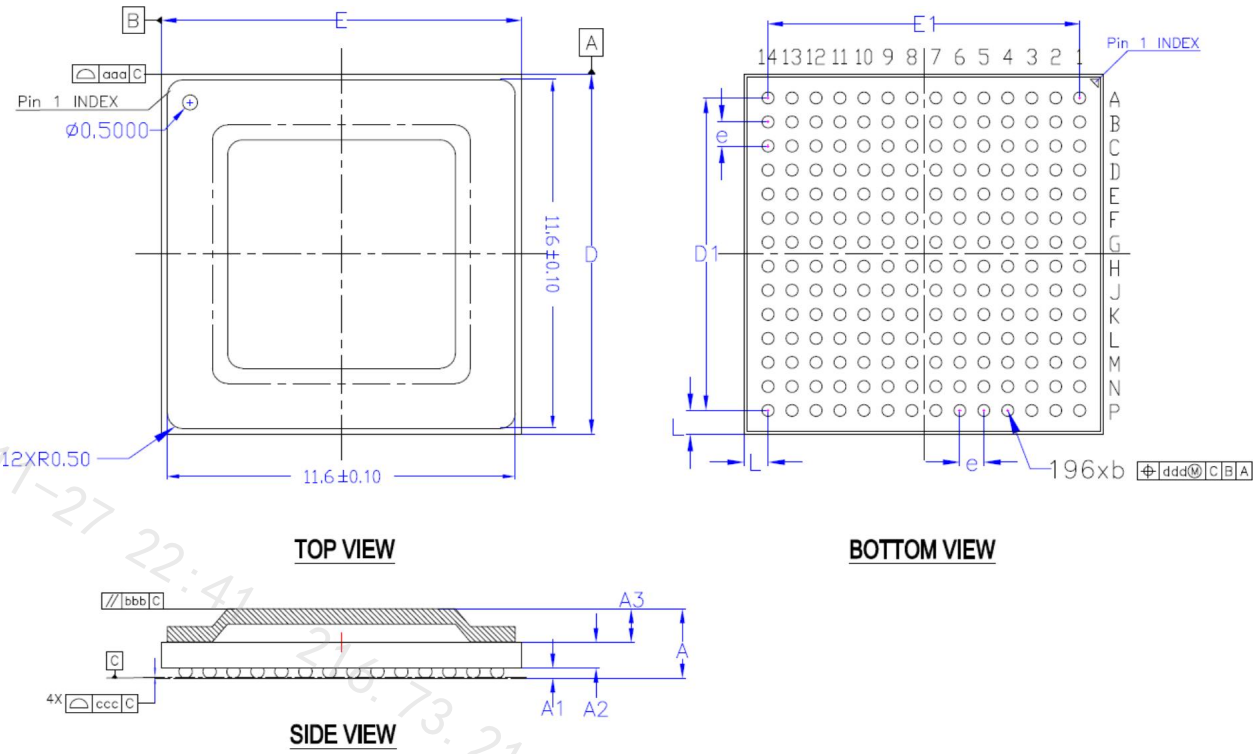

图 23 封装尺寸

Dimensional Ref.

表 15 封装尺寸（单位：mm）

REF.	Min.	Nom.	Max.
A	2.13	2.32	2.51
A1	0.30	0.35	0.40
A2	0.76	0.85	0.94
A3	1.07	1.12	1.17
D	11.9	12.0	12.1
E	11.9	12.0	12.1
D1		10.4 BSC	
E1		10.4 BSC	
L		0.8 REF	
e		0.8 BSC	
b	0.40	0.45	0.50
	Tol. of Form	& Position	
aaa		0.10	
bbb		0.10	
ccc		0.20	
ddd		0.05	

Notes:
1. All Dimensions are in Millimeters (Angles in Degrees).
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

10. 说明

如欲了解更多的产品及及公司信息，请登录网站：https://www.chiphelps.com

11. 本文档中的信息如有变更，恕不另行通知

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文档版本	修订日期	内容描述
V1.0	2026-11-20	初版

2026-11-27 22:41 216.73.216.43